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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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SCHWEGMAN, LUNDBERG & WOESSNER, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER

DICKEY, THOMAS L

ART UNIT	PAPER NUMBER
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2826

MAIL DATE	DELIVERY MODE
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04/09/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.		Applicant(s)	
	10/612,793		BHATTACHARYYA, ARUP	
	Examiner		Art Unit	
	Thomas L. Dickey		2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period **will** apply and **will** expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply **will**, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 December 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-79 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-79 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

/Thomas L. Dickey/ Primary Examiner Art Unit 2826
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Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>12/27/07</u> . | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
5) <input type="checkbox"/> Notice of Informal Patent Application
6) <input type="checkbox"/> Other: _____. |
|--|--|

DETAILED ACTION

1. The amendment filed on 12/27/07 has been entered.

Response to Arguments

2. Shortly after the last action mailed, this Office published the *Examination Guidelines for Determining Obviousness Under 35 U.S.C. 103 in View of the Supreme Court Decision in KSR International Co. v. Teleflex Inc.* It is believed Applicant may better understand the obviousness of the current claims with the aid of a rejection that follows the framework of one of the rationales set forth in the *Examination Guidelines*. For this reason, a new non-final Action has been issued which closely follows one of the rationales set forth in the *Examination Guidelines*.

Applicant's arguments with respect to claims 1-79 have been considered but are moot in view of the new ground(s) of rejection.

Information Disclosure Statement

3. The Information Disclosure Statement filed on 12/27/07 has been considered.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

A. Claims 1-79 are rejected under 35 U.S.C. 103(a) as being unpatentable over HORCH ET AL. (6,965,129) in view of BABA (5,686,739). In the examiner's opinion, this/these claim(s) would have been obvious according to one of the rationales expressed in the *Examination Guidelines for Determining Obviousness Under 35 U.S.C.*

Art Unit: 2826

103 in View of the Supreme Court Decision in *KSR International Co. v. Teleflex Inc.*, as published at 72 Federal Register 57526 et seq.¹ (10/10/2007).

The Guidelines explain that an invention that would have been obvious to a person of ordinary skill at the time of the invention is not patentable. The Guidelines point out that, as reiterated by the Supreme Court in KSR, the framework for the objective analysis for determining obviousness under 35 U.S.C. 103 is stated in *Graham v. John Deere Co.* Obviousness is a question of law based on underlying factual inquiries. The factual inquiries enunciated by the Court are as follows:

- (1) Determining the scope and content of the prior art;
- (2) Ascertaining the differences between the claimed invention and the prior art, and
- (3) Resolving the level of ordinary skill in the pertinent art.

Examining this last factor first, it is noted that any obviousness rejection should include, either explicitly or implicitly in view of the prior art applied, an indication of the level of ordinary skill. This is an essential finding because (as the Guidelines point out) a finding as to the level of ordinary skill may be used as a partial basis for a resolution of the issue of obviousness. The person of ordinary skill in the art is a hypothetical person who is presumed to have known the relevant art at the time of the invention. Factors that may be considered in determining the level of ordinary skill in the art include:

- (1) "Type of problems encountered in the art;"
- (2) "prior art solutions to those problems;"
- (3) "rapidity with which innovations are made;"
- (4) "sophistication of the technology;" and
- (5) "educational level of active workers in the field."

In a given case, not every factor may be present, or one or more factors may predominate.

In the present case, Applicant has presented claims to a device classified in Class 257 (Semiconductor Devices). The types of problems encountered in Class 257 typically are highly complex, involving questions of electrodynamics, thermodynamics, crystallography, and quantum mechanics. Prior art solutions to the problems presented in

¹ Available at <http://www.uspto.gov/web/offices/com/sol/notices/72fr57526.pdf>

Art Unit: 2826

this field demonstrate thinking of the highest order. Many prior art solutions in this field have won Nobel prizes. Past Nobel prizewinners for Class 257 innovations include John Bardeen, William Shockley, Jack Kilby, Leo Esaki, Nick Basow, Zhores Alferov, Pierre-Gilles de Gennes, and probably a half dozen more this writer has forgotten. Innovations in Class 257 are made with extremely high rapidity (see, e.g. "Moore's Law"). Technology used to make and practice inventions in this field are highly sophisticated. Some "fabs" (as those of skill in the art call the factories for making these devices) now cost in excess of one billion dollars each, and perform literally hundreds of billions of operations per hour. Finally, the educational level of active workers in this field is extremely high – Ph.D.s are common, and a bachelor's degree in engineering is the absolute minimum educational level of workers in this field.

In short, the level of ordinary skill in this field is extremely high. In *KSR*, the Supreme Court cautioned, "A person of ordinary skill is also a person of ordinary creativity." *KSR Int'l Co. v. Teleflex Inc.*, 127 S.Ct. 1727, 1742, 82 USPQ2d 1385, 1397 (2007). Had the Court taken a look at the people who have practiced the semiconductor art in the past and the variety of extraordinarily valuable (from lifestyle-changing, such as high-speed communications and computing, to handy devices such as iPods and cell-phones) and difficult solutions to challenging problems those people have accomplished, the Court might easily have said that in the semiconductor art the person of ordinary skill is a person of extraordinary creativity.

Next, we consider the first and second factual findings required by *Graham*. With regard to claims 1-5, the scope and content of the prior art includes, in the Horch et al. disclosure, a description of a memory cell, comprising an access transistor 350 or 360 having a floating node 339 or 939, the floating node 339 or 939 to store a charge indicative of a memory state of the memory cell; and a gate-controlled N-P-N-P thyristor 330 or 930 exhibiting Negative Differential Resistance (NDR) behavior connected between the floating node 339 or 939 and a diode reference potential line 440 (see fig. 4), the N-P-N-P thyristor 330 or 930 having a junction diode including an anode 332 or 932 and a cathode 338 or 938, wherein the cathode 338 or 938 of the diode 330 or 930 may be connected to the floating node 339 or 939 of the access transistor 350 or 360 and the access transistor 350 or 360 may be formed in either a bulk semiconductor (note figures

Art Unit: 2826

3 and 9) structure or a semiconductor-on-insulator (note figures 1 and 2) structure. Note figures 1-4,9, column 6 lines 42-67, column 7, column 8 lines 31-67, and column 10 lines 39-67 of Horch et al. Note, column 11 lines 41-57, that Horch et al. did not explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. “[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.” Ex parte CAROLYN RAMSEY CATAN, 83 USPQ2d 1569, 1573 (Bd. Pat. App. & Int. 2007 PRECEDENTIAL), quoting KSR, 127 S.Ct. at 1741, 82 USPQ2d at 1396.

The difference between the prior art memory cell disclosed by Horch et al. and the claimed device is that, where the claims 1-5 require an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode, Horch et al.’s memory cell includes an N-P-N-P negative resistance thyristor. However, Baba discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Baba. The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claims 1-5 by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for Horch et al.’s N-P-N-P negative resistance thyristor?

To base a claim rejection on the framework of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

- (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;
- (2) a finding that the substituted components and their functions were known in the art;
- (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and

Art Unit: 2826

(4) whatever additional findings based on the Graham factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Horch et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode) for other components (an N-P-N-P negative resistance thyristor). Baba discloses that the substituted components and their functions were known in the art. Further, Baba discloses that those of skill in the art were familiar with a method of combining the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode with a memory cell very similar to Horch et al.'s memory cell. From the similarities between the I/V response curves of Baba's P-I-N negative resistance diode and the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell, one of skill in the art would have been able to conclude that Baba's P-I-N negative resistance diode would have been substitutable for the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell) that Baba's P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Horch et al.'s memory cell, and that in said combination Horch et al.'s memory cell would continue functioning in the manner disclosed by Horch et al. It would therefore have been obvious to a person having skill in the art to modify Horch et al.'s memory cell by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell.

With regard to claim 6, the scope and content of the prior art includes, in the Horch et al. disclosure, a description of a memory cell, comprising an access transistor 350 or 360 having a first diffusion region 356 (fig. 3) or 364 (fig. 9) connected to a bit line 430 or 435, and a second diffusion region 354 (fig. 3) or 356 (fig. 9), the second diffusion region 354 (fig. 3) or 356 (fig. 9) to store a charge indicative of a memory state of the memory cell; a Negative Differential Resistance (NDR) thyristor including junction diode

Art Unit: 2826

330 or 930 connected between the second diffusion region 354 (fig. 3) or 356 (fig. 9) and a diode reference potential line 440 (see fig. 4), the diode 330 or 930 including an anode 332 or 932; a cathode 338 or 938; and a diode gate 913. Note figures 1-4,9, column 6 lines 42-67, column 7, column 8 lines 31-67, and column 10 lines 39-67 of Horch et al. Note, column 11 lines 41-57, that Horch et al. did not explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. “[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.” CATAN, 83 USPQ2d at 1573, quoting KSR, 127 S.Ct. at 1741, 82 USPQ2d at 1396.

The difference between the prior art memory cell disclosed by Horch et al. and the claimed device is that, where claim 6 requires an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode, and operatively positioned to enhance switching performance, Horch et al.’s memory cell includes an N-P-N-P negative resistance thyristor. However, Baba discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode, and operatively positioned to enhance switching performance. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Baba. The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claim 6 by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode, and operatively positioned to enhance switching performance taught by Baba for Horch et al.’s N-P-N-P negative resistance thyristor?

To base a claim rejection on the framework of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

- (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;

Art Unit: 2826

- (2) a finding that the substituted components and their functions were known in the art;
- (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and
- (4) whatever additional findings based on the Graham factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Horch et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (a NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode, and operatively positioned to enhance switching performance) for other components (a N-P-N-P negative resistance thyristor). Baba discloses that the substituted components and their functions were known in the art. Further, Baba discloses that those of skill in the art were familiar with a method of combining the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode, and operatively positioned to enhance switching performance, with a memory cell very similar to Horch et al.'s memory cell. From the similarities between the I/V response curves of Baba's P-I-N negative resistance diode and the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell, one of skill in the art would have been able to conclude that Baba's P-I-N negative resistance diode would have been substitutable for the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell) that Baba's P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Horch et al.'s memory cell, and that in said combination Horch et al.'s memory cell would continue functioning in the manner disclosed by Horch et al. It would therefore have been obvious to a person having skill in the art to modify Horch et al.'s memory cell by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode, and operatively positioned to enhance switching performance taught by Baba for the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell.

With regard to claim 7, the scope and content of the prior art includes, in the Horch et al. disclosure, a description of a memory cell, comprising an n-channel access tran-

Art Unit: 2826

sistor 350 or 360 on a bulk semiconductor (note figures 3 and 9) substrate, the n-channel access transistor 350 or 360 having a n-type first diffusion region 356 (fig. 3) or 364 (fig. 9) connected to a bit line 430 or 435 and an n-type second diffusion region 354 (fig. 3) or 356 (fig. 9), the n-type second diffusion region 354 (fig. 3) or 356 (fig. 9) to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) 330 or 930 including an n/p junction diode having an n-type anode 332 or 932 connected to a diode reference potential line 440 (see fig. 4) and a p-type cathode 338 or 938 in contact with the n-type second diffusion region 354 (fig. 3) or 356 (fig. 9). Note figures 1-4,9, column 6 lines 42-67, column 7, column 8 lines 31-67, and column 10 lines 39-67 of Horch et al. Note, column 11 lines 41-57, that Horch et al. did not explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. “[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.” CATAN, 83 USPQ2d at 1573, quoting KSR, 127 S.Ct. at 1741, 82 USPQ2d at 1396.

The difference between the prior art memory cell disclosed by Horch et al. and the claimed device is that, where the claim(s) requires an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode, Horch et al.’s memory cell includes an N-P-N-P negative resistance thyristor. However, Baba discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Baba. The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claim 7 by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for Horch et al.’s N-P-N-P negative resistance thyristor?

Art Unit: 2826

To base a claim rejection on the framework of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

- (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;
- (2) a finding that the substituted components and their functions were known in the art;
- (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and
- (4) whatever additional findings based on the Graham factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Horch et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode) for other components (a N-P-N-P negative resistance thyristor). Baba discloses that the substituted components and their functions were known in the art. Further, Baba discloses that those of skill in the art were familiar with a method of combining the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode with a memory cell very similar to Horch et al.'s memory cell. From the similarities between the I/V response curves of Baba's P-I-N negative resistance diode and the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell, one of skill in the art would have been able to conclude that Baba's P-I-N negative resistance diode would have been substitutable for the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell) that Baba's P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Horch et al.'s memory cell, and that in said combination Horch et al.'s memory cell would continue functioning in the manner disclosed by Horch et al. It would therefore have been obvious to a person having skill in the art to modify Horch et al.'s memory cell by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the

Art Unit: 2826

NDR diode taught by Baba for the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell.

With regard to claim 8, the scope and content of the prior art includes, in the Horch et al. disclosure, a description of a memory cell, comprising a p-channel access transistor 350 or 360 on a bulk semiconductor (note figures 3 and 9) substrate, the p-channel access transistor 350 or 360 having a p-type first diffusion region 356 (fig. 3) or 364 (fig. 9) connected to a bit line 430 or 435 and a p-type second diffusion region 354 (fig. 3) or 356 (fig. 9), the p-type second diffusion region 354 (fig. 3) or 356 (fig. 9) to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) 330 or 930 including an n/p junction diode having an n-type anode 332 or 932 connected to a diode reference potential line 440 (see fig. 4) and a p-type cathode 338 or 938 formed with the n-type second diffusion region 354 (fig. 3) or 356 (fig. 9). Note figures 1-4,9, column 6 lines 42-67, column 7, column 8 lines 31-67, and column 10 lines 39-67 of Horch et al. Note, column 11 lines 41-57, that Horch et al. did not explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. "[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." CATAN, 83 USPQ2d at 1573, quoting KSR, 127 S.Ct. at 1741, 82 USPQ2d at 1396.

The difference between the prior art memory cell disclosed by Horch et al. and the claimed device is that, where the claim(s) requires an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode, Horch et al.'s memory cell includes an N-P-N-P negative resistance thyristor. However, Baba discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Baba. The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the

Art Unit: 2826

invention of claim 8 by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for Horch et al.'s N-P-N-P negative resistance thyristor?

To base a claim rejection on the framework of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

- (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;
- (2) a finding that the substituted components and their functions were known in the art;
- (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and
- (4) whatever additional findings based on the Graham factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Horch et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode) for other components (an N-P-N-P negative resistance thyristor). Baba discloses that the substituted components and their functions were known in the art. Further, Baba discloses that those of skill in the art were familiar with a method of combining the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode with a memory cell very similar to Horch et al.'s memory cell. From the similarities between the I/V response curves of Baba's P-I-N negative resistance diode and the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell, one of skill in the art would have been able to conclude that Baba's P-I-N negative resistance diode would have been substitutable for the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell) that Baba's P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Horch et al.'s memory cell, and that in said combination Horch et al.'s memory cell would continue functioning in the manner disclosed by Horch et al. It would therefore have been obvious to a person having skill

Art Unit: 2826

in the art to modify Horch et al.'s memory cell by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell.

With regard to claim 9, the scope and content of the prior art includes, in the Horch et al. disclosure, a description of a memory cell, comprising an n-channel access transistor 350 or 360 on a bulk semiconductor (note figures 3 and 9) substrate, the p-channel access transistor 350 or 360 having a n-type first diffusion region 356 (fig. 3) or 364 (fig. 9) connected to a bit line 430 or 435 and an n-type second diffusion region 354 (fig. 3) or 356 (fig. 9), the n-type second diffusion region 354 (fig. 3) or 356 (fig. 9) to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) 330 or 930 including a p/n junction diode having a p-type anode 332 or 932 connected to a diode reference potential line 440 (see fig. 4) and an n-type cathode 338 or 938 formed with the n-type second diffusion region 354 (fig. 3) or 356 (fig. 9). Note figures 1-4,9, column 6 lines 42-67, column 7, column 8 lines 31-67, and column 10 lines 39-67 of Horch et al. Note, column 11 lines 41-57, that Horch et al. did not explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. "[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." CATAN, 83 USPQ2d at 1573, quoting KSR, 127 S.Ct. at 1741, 82 USPQ2d at 1396.

The difference between the prior art memory cell disclosed by Horch et al. and the claimed device is that, where the claim(s) requires an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode, Horch et al.'s memory cell includes an N-P-N-P negative resistance thyristor. However, Baba discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Baba.

Art Unit: 2826

The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claim 9 by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for Horch et al.'s N-P-N-P negative resistance thyristor?

To base a claim rejection on the framework of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

- (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;
- (2) a finding that the substituted components and their functions were known in the art;
- (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and
- (4) whatever additional findings based on the Graham factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Horch et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode) for other components (an N-P-N-P negative resistance thyristor). Baba discloses that the substituted components and their functions were known in the art. Further, Baba discloses that those of skill in the art were familiar with a method of combining the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode with a memory cell very similar to Horch et al.'s memory cell. From the similarities between the I/V response curves of Baba's P-I-N negative resistance diode and the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell, one of skill in the art would have been able to conclude that Baba's P-I-N negative resistance diode would have been substitutable for the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell) that Baba's P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Horch et al.'s memory cell, and that

Art Unit: 2826

in said combination Horch et al.'s memory cell would continue functioning in the manner disclosed by Horch et al. It would therefore have been obvious to a person having skill in the art to modify Horch et al.'s memory cell by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell.

With regard to claim 10, the scope and content of the prior art includes, in the Horch et al. disclosure, a description of a memory cell, comprising a p-channel access transistor 350 or 360 on a bulk semiconductor (note figures 3 and 9) substrate, the p-channel access transistor 350 or 360 having a p-type first diffusion region 356 (fig. 3) or 364 (fig. 9) connected to a bit line 430 or 435 and a p-type second diffusion region 354 (fig. 3) or 356 (fig. 9), the p-type second diffusion region 354 (fig. 3) or 356 (fig. 9) to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) 330 or 930 including a p/n junction diode having a p-type anode 332 or 932 connected to a diode reference potential line 440 (see fig. 4) and an n-type cathode 338 or 938 in contact with the p-type second diffusion region 354 (fig. 3) or 356 (fig. 9). Note figures 1-4,9, column 6 lines 42-67, column 7, column 8 lines 31-67, and column 10 lines 39-67 of Horch et al. Note, column 11 lines 41-57, that Horch et al. did not explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. "[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." CATAN, 83 USPQ2d at 1573, quoting KSR, 127 S.Ct. at 1741, 82 USPQ2d at 1396.

The difference between the prior art memory cell disclosed by Horch et al. and the claimed device is that, where the claim(s) requires an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode, Horch et al.'s memory cell includes an N-P-N-P negative resistance thyristor. However, Baba discloses a P-I-N negative resistance diode 10 with an intrinsic re-

Art Unit: 2826

gion 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Baba. The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claim 10 by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for Horch et al.'s N-P-N-P negative resistance thyristor?

To base a claim rejection on the framework of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

- (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;
- (2) a finding that the substituted components and their functions were known in the art;
- (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and
- (4) whatever additional findings based on the Graham factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Horch et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode) for other components (a N-P-N-P negative resistance thyristor). Baba discloses that the substituted components and their functions were known in the art. Further, Baba discloses that those of skill in the art were familiar with a method of combining the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode with a memory cell very similar to Horch et al.'s memory cell. From the similarities between the I/V response curves of Baba's P-I-N negative resistance diode and the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell, one of skill in the art would have been able to conclude that Baba's P-I-N negative resistance diode would have been substitutable for the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell)

Art Unit: 2826

that Baba's P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Horch et al.'s memory cell, and that in said combination Horch et al.'s memory cell would continue functioning in the manner disclosed by Horch et al. It would therefore have been obvious to a person having skill in the art to modify Horch et al.'s memory cell by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell.

With regard to claim 11, the scope and content of the prior art includes, in the Horch et al. disclosure, a description of a memory cell, comprising an access transistor 350 or 360 on a bulk semiconductor (note figures 3 and 9) substrate, the access transistor 350 or 360 having a first diffusion region 356 (fig. 3) or 364 (fig. 9) connected to a bit line 430 or 435 and a second diffusion region 354 (fig. 3) or 356 (fig. 9), the second diffusion region 354 (fig. 3) or 356 (fig. 9) to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) thyristor including junction diode 330 or 930 connected between the second diffusion region 354 (fig. 3) or 356 (fig. 9) of the access transistor 350 or 360 and a diode reference potential line 440 (see fig. 4), the diode 330 or 930 having an anode 332 or 932 and a cathode 338 or 938, the diode 330 or 930 being laterally oriented over the access transistor 350 or 360. Note figures 1-4,9, column 6 lines 42-67, column 7, column 8 lines 31-67, and column 10 lines 39-67 of Horch et al. Note, column 11 lines 41-57, that Horch et al. did not explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. "[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." CATAN, 83 USPQ2d at 1573, quoting KSR, 127 S.Ct. at 1741, 82 USPQ2d at 1396.

The difference between the prior art memory cell disclosed by Horch et al. and the claimed device is that, where the claim(s) requires an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the

Art Unit: 2826

NDR diode, Horsch et al.'s memory cell includes an N-P-N-P negative resistance thyristor. However, Baba discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Baba. The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claim 11 by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for Horsch et al.'s N-P-N-P negative resistance thyristor?

To base a claim rejection on the framework of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

- (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;
- (2) a finding that the substituted components and their functions were known in the art;
- (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and
- (4) whatever additional findings based on the Graham factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Horsch et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode) for other components (a N-P-N-P negative resistance thyristor). Baba discloses that the substituted components and their functions were known in the art. Further, Baba discloses that those of skill in the art were familiar with a method of combining the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode with a memory cell very similar to Horsch et al.'s memory cell. From the similarities between the I/V response curves of Baba's P-I-N negative resistance diode and the N-P-N-P negative resistance thyristor of Horsch et al.'s memory cell, one of skill in the art would have been able to conclude that Baba's P-I-N negative resistance diode would have been substitutable for the N-P-N-P negative resistance thyristor of Horsch et al.'s memory cell. One of skill in

Art Unit: 2826

the art would have had reason to predict (based on the similarity of its functioning to the functioning of the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell) that Baba's P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Horch et al.'s memory cell, and that in said combination Horch et al.'s memory cell would continue functioning in the manner disclosed by Horch et al. It would therefore have been obvious to a person having skill in the art to modify Horch et al.'s memory cell by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell.

With regard to claim 12, the scope and content of the prior art includes, in the Horch et al. disclosure, a description of a memory cell, comprising an access transistor 350 or 360 on a bulk semiconductor (note figures 3 and 9) substrate, the access transistor 350 or 360 having a first diffusion region 356 (fig. 3) or 364 (fig. 9) connected to a bit line 430 or 435 and a second diffusion region 354 (fig. 3) or 356 (fig. 9), the second diffusion region 354 (fig. 3) or 356 (fig. 9) to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) thyristor including junction diode 330 or 930 connected between the second diffusion region 354 (fig. 3) or 356 (fig. 9) of the access transistor 350 or 360 and a diode reference potential line 440 (see fig. 4), the diode 330 or 930 having an anode 332 or 932 and a cathode 338 or 938, the diode 330 or 930 being vertically oriented over the access transistor 350 or 360. Note figures 1-4,9, column 6 lines 42-67, column 7, column 8 lines 31-67, and column 10 lines 39-67 of Horch et al. Note, column 11 lines 41-57, that Horch et al. did not explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. "[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." CATAN, 83 USPQ2d at 1573, quoting KSR, 127 S.Ct. at 1741, 82 USPQ2d at 1396.

Art Unit: 2826

The difference between the prior art memory cell disclosed by Horch et al. and the claimed device is that, where the claim(s) requires an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode, Horch et al.'s memory cell includes an N-P-N-P negative resistance thyristor. However, Baba discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Baba. The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claim 12 by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for Horch et al.'s N-P-N-P negative resistance thyristor?

To base a claim rejection on the framework of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

- (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;
- (2) a finding that the substituted components and their functions were known in the art;
- (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and
- (4) whatever additional findings based on the Graham factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Horch et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode) for other components (a N-P-N-P negative resistance thyristor). Baba discloses that the substituted components and their functions were known in the art. Further, Baba discloses that those of skill in the art were familiar with a method of combining the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode with a memory cell very similar to Horch et al.'s memory cell. From the similarities between the I/V response curves of Baba's P-I-N negative resistance diode and the N-P-N-P negative resistance

Art Unit: 2826

thyristor of Horch et al.'s memory cell, one of skill in the art would have been able to conclude that Baba's P-I-N negative resistance diode would have been substitutable for the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell) that Baba's P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Horch et al.'s memory cell, and that in said combination Horch et al.'s memory cell would continue functioning in the manner disclosed by Horch et al. It would therefore have been obvious to a person having skill in the art to modify Horch et al.'s memory cell by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell.

With regard to claim 13, the scope and content of the prior art includes, in the Horch et al. disclosure, a description of a memory cell, comprising an n-channel access transistor 350 or 360 on a semiconductor-on-insulator (note figures 1 and 2) substrate, the n-channel access transistor 350 or 360 having a floating body (part of second diffusion 2) and a n-type first diffusion region 356 (fig. 3) or 364 (fig. 9) connected to a bit line 430 or 435 and an n-type second diffusion region 354 (fig. 3) or 356 (fig. 9), the n-type second diffusion region 354 (fig. 3) or 356 (fig. 9) to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) 330 or 930 including an n/p junction diode having an n-type anode 332 or 932 connected to a diode reference potential line 440 (see fig. 4) and a p-type cathode 338 or 938 in contact with the n-type second diffusion region 354 (fig. 3) or 356 (fig. 9), said cell being reasonable capable, should circumstances arise, of performing the function of enhancing diode 330 or 930 switching with intentionally-generated charges in the floating body of the access transistor 350 or 360. Note figures 1-4,9, column 6 lines 42-67, column 7, column 8 lines 31-67, and column 10 lines 39-67 of Horch et al. Note, column 11 lines 41-57, that Horch et al. did not explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been

Art Unit: 2826

suggested to one of skill in the art by the explicit teachings. “[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.” CATAN, 83 USPQ2d at 1573, quoting KSR, 127 S.Ct. at 1741, 82 USPQ2d at 1396.

The difference between the prior art memory cell disclosed by Horch et al. and the claimed device is that, where the claim(s) requires an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode, Horch et al.’s memory cell includes an N-P-N-P negative resistance thyristor. However, Baba discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Baba. The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claim 13 by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for Horch et al.’s N-P-N-P negative resistance thyristor?

To base a claim rejection on the framework of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

- (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;
- (2) a finding that the substituted components and their functions were known in the art;
- (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and
- (4) whatever additional findings based on the Graham factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Horch et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode) for other components (an N-P-N-P negative resistance thyristor). Baba discloses that the substituted components and their functions were known

Art Unit: 2826

in the art. Further, Baba discloses that those of skill in the art were familiar with a method of combining the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode with a memory cell very similar to Horch et al.'s memory cell. From the similarities between the I/V response curves of Baba's P-I-N negative resistance diode and the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell, one of skill in the art would have been able to conclude that Baba's P-I-N negative resistance diode would have been substitutable for the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell) that Baba's P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Horch et al.'s memory cell, and that in said combination Horch et al.'s memory cell would continue functioning in the manner disclosed by Horch et al. It would therefore have been obvious to a person having skill in the art to modify Horch et al.'s memory cell by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell.

With regard to claim 14, the scope and content of the prior art includes, in the Horch et al. disclosure, a description of a memory cell, comprising a p-channel access transistor 350 or 360 on a semiconductor-on-insulator (note figures 1 and 2) substrate, the p-channel access transistor 350 or 360 having a floating body (part of second diffusion 2) and a p-type first diffusion region 356 (fig. 3) or 364 (fig. 9) connected to a bit line 430 or 435 and a p-type second diffusion region 354 (fig. 3) or 356 (fig. 9), the p-type second diffusion region 354 (fig. 3) or 356 (fig. 9) to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) 330 or 930 including an n/p junction diode having an n-type anode 332 or 932 connected to a diode reference potential line 440 (see fig. 4) and a p-type cathode 338 or 938 in contact with the n-type second diffusion region 354 (fig. 3) or 356 (fig. 9), said cell being reasonable capable, should circumstances arise, of performing the function of enhancing diode 330 or 930 switching with intentionally-generated charges in the floating body of the access

Art Unit: 2826

transistor 350 or 360. Note figures 1-4, 9, column 6 lines 42-67, column 7, column 8 lines 31-67, and column 10 lines 39-67 of Horsch et al. Note, column 11 lines 41-57, that Horsch et al. did not explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or side-ways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. “[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.” CATAN, 83 USPQ2d at 1573, quoting KSR, 127 S.Ct. at 1741, 82 USPQ2d at 1396.

The difference between the prior art memory cell disclosed by Horsch et al. and the claimed device is that, where the claim(s) requires an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode, Horsch et al.’s memory cell includes an N-P-N-P negative resistance thyristor. However, Baba discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Baba. The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claim 14 by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for Horsch et al.’s N-P-N-P negative resistance thyristor?

To base a claim rejection on the framework of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

- (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;
- (2) a finding that the substituted components and their functions were known in the art;
- (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and
- (4) whatever additional findings based on the Graham factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Horch et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode) for other components (an N-P-N-P negative resistance thyristor). Baba discloses that the substituted components and their functions were known in the art. Further, Baba discloses that those of skill in the art were familiar with a method of combining the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode with a memory cell very similar to Horch et al.'s memory cell. From the similarities between the I/V response curves of Baba's P-I-N negative resistance diode and the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell, one of skill in the art would have been able to conclude that Baba's P-I-N negative resistance diode would have been substitutable for the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell) that Baba's P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Horch et al.'s memory cell, and that in said combination Horch et al.'s memory cell would continue functioning in the manner disclosed by Horch et al. It would therefore have been obvious to a person having skill in the art to modify Horch et al.'s memory cell by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell.

With regard to claim 15, the scope and content of the prior art includes, in the Horch et al. disclosure, a description of a memory cell, comprising an n-channel access transistor 350 or 360 on a semiconductor-on-insulator (note figures 1 and 2) substrate, the p-channel access transistor 350 or 360 having a floating body (part of second diffusion 2) and a n-type first diffusion region 356 (fig. 3) or 364 (fig. 9) connected to a bit line 430 or 435 and an n-type second diffusion region 354 (fig. 3) or 356 (fig. 9), the n-type second diffusion region 354 (fig. 3) or 356 (fig. 9) to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) 330 or 930 in-

Art Unit: 2826

cluding a p/n junction diode having a p-type anode 332 or 932 connected to a diode reference potential line 440 (see fig. 4) and an n-type cathode 338 or 938 formed with the n-type second diffusion region 354 (fig. 3) or 356 (fig. 9), said cell being reasonable capable, should circumstances arise, of performing the function of enhancing diode 330 or 930 switching with intentionally-generated charges in the floating body of the access transistor 350 or 360. Note figures 1-4,9, column 6 lines 42-67, column 7, column 8 lines 31-67, and column 10 lines 39-67 of Horch et al. Note, column 11 lines 41-57, that Horch et al. did not explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. "[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." CATAN, 83 USPQ2d at 1573, quoting KSR, 127 S.Ct. at 1741, 82 USPQ2d at 1396.

The difference between the prior art memory cell disclosed by Horch et al. and the claimed device is that, where the claim(s) requires an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode, Horch et al.'s memory cell includes an N-P-N-P negative resistance thyristor. However, Baba discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Baba. The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claim 15 by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for Horch et al.'s N-P-N-P negative resistance thyristor?

To base a claim rejection on the framework of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

- (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;

Art Unit: 2826

- (2) a finding that the substituted components and their functions were known in the art;
- (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and
- (4) whatever additional findings based on the Graham factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Horch et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode) for other components (an N-P-N-P negative resistance thyristor). Baba discloses that the substituted components and their functions were known in the art. Further, Baba discloses that those of skill in the art were familiar with a method of combining the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode with a memory cell very similar to Horch et al.'s memory cell. From the similarities between the I/V response curves of Baba's P-I-N negative resistance diode and the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell, one of skill in the art would have been able to conclude that Baba's P-I-N negative resistance diode would have been substitutable for the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell) that Baba's P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Horch et al.'s memory cell, and that in said combination Horch et al.'s memory cell would continue functioning in the manner disclosed by Horch et al. It would therefore have been obvious to a person having skill in the art to modify Horch et al.'s memory cell by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell.

With regard to claim 16, the scope and content of the prior art includes, in the Horch et al. disclosure, a description of a memory cell, comprising a p-channel access transistor 350 or 360 on a semiconductor-on-insulator (note figures 1 and 2) substrate, the p-channel access transistor 350 or 360 having a floating body (part of second diffusion 2)

Art Unit: 2826

and a p-type first diffusion region 356 (fig. 3) or 364 (fig. 9) connected to a bit line 430 or 435 and a p-type second diffusion region 354 (fig. 3) or 356 (fig. 9), the p-type second diffusion region 354 (fig. 3) or 356 (fig. 9) to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) 330 or 930 including a p/n junction diode having a p-type anode 332 or 932 connected to a diode reference potential line 440 (see fig. 4) and an n-type cathode 338 or 938 formed with the n-type second diffusion region 354 (fig. 3) or 356 (fig. 9), said cell being reasonable capable, should circumstances arise, of performing the function of enhancing diode 330 or 930 switching with intentionally-generated charges in the floating body of the access transistor 350 or 360. Note figures 1-4,9, column 6 lines 42-67, column 7, column 8 lines 31-67, and column 10 lines 39-67 of Horch et al. Note, column 11 lines 41-57, that Horch et al. did not explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. “[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.” CATAN, 83 USPQ2d at 1573, quoting KSR, 127 S.Ct. at 1741, 82 USPQ2d at 1396.

The difference between the prior art memory cell disclosed by Horch et al. and the claimed device is that, where the claim(s) requires an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode, Horch et al.’s memory cell includes an N-P-N-P negative resistance thyristor. However, Baba discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Baba. The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claim 16 by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for Horch et al.’s N-P-N-P negative resistance thyristor?

Art Unit: 2826

To base a claim rejection on the framework of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

- (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;
- (2) a finding that the substituted components and their functions were known in the art;
- (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and
- (4) whatever additional findings based on the Graham factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Horch et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode) for other components (an N-P-N-P negative resistance thyristor). Baba discloses that the substituted components and their functions were known in the art. Further, Baba discloses that those of skill in the art were familiar with a method of combining the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode with a memory cell very similar to Horch et al.'s memory cell. From the similarities between the I/V response curves of Baba's P-I-N negative resistance diode and the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell, one of skill in the art would have been able to conclude that Baba's P-I-N negative resistance diode would have been substitutable for the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell) that Baba's P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Horch et al.'s memory cell, and that in said combination Horch et al.'s memory cell would continue functioning in the manner disclosed by Horch et al. It would therefore have been obvious to a person having skill in the art to modify Horch et al.'s memory cell by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state

Art Unit: 2826

of the NDR diode taught by Baba for the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell.

With regard to claim 17, the scope and content of the prior art includes, in the Horch et al. disclosure, a description of a memory cell, comprising an access transistor 350 or 360 on a semiconductor-on-insulator (note figures 1 and 2) substrate, the access transistor 350 or 360 having a floating body (part of second diffusion 2) and a first diffusion region 356 (fig. 3) or 364 (fig. 9) connected to a bit line 430 or 435 and a second diffusion region 354 (fig. 3) or 356 (fig. 9), the second diffusion region 354 (fig. 3) or 356 (fig. 9) to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) thyristor including junction diode 330 or 930 connected between the second diffusion region 354 (fig. 3) or 356 (fig. 9) of the access transistor 350 or 360 and a diode reference potential line 440 (see fig. 4), the diode 330 or 930 having an anode 332 or 932 and an n-type cathode 338 or 938 formed with the n-type second diffusion region 354 (fig. 3) or 356 (fig. 9), said cell being reasonable capable, should circumstances arise, of performing the function of enhancing diode 330 or 930 switching with intentionally-generated charges in the floating body of the access transistor 350 or 360. Note figures 1-4,9, column 6 lines 42-67, column 7, column 8 lines 31-67, and column 10 lines 39-67 of Horch et al. Note, column 11 lines 41-57, that Horch et al. did not explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. "[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." CATAN, 83 USPQ2d at 1573, quoting KSR, 127 S.Ct. at 1741, 82 USPQ2d at 1396.

The difference between the prior art memory cell disclosed by Horch et al. and the claimed device is that, where the claim(s) requires an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode, Horch et al.'s memory cell includes an N-P-N-P negative resistance thyristor. However, Baba discloses a P-I-N negative resistance diode 10 with an intrinsic re-

Art Unit: 2826

gion 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Baba. The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claim 17 by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for Horch et al.'s N-P-N-P negative resistance thyristor?

To base a claim rejection on the framework of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

- (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;
- (2) a finding that the substituted components and their functions were known in the art;
- (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and
- (4) whatever additional findings based on the Graham factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Horch et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode) for other components (an N-P-N-P negative resistance thyristor). Baba discloses that the substituted components and their functions were known in the art. Further, Baba discloses that those of skill in the art were familiar with a method of combining the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode with a memory cell very similar to Horch et al.'s memory cell. From the similarities between the I/V response curves of Baba's P-I-N negative resistance diode and the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell, one of skill in the art would have been able to conclude that Baba's P-I-N negative resistance diode would have been substitutable for the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the N-P-N-P negative resistance thyristor of Horch et al.'s

memory cell) that Baba's P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Horch et al.'s memory cell, and that in said combination Horch et al.'s memory cell would continue functioning in the manner disclosed by Horch et al. It would therefore have been obvious to a person having skill in the art to modify Horch et al.'s memory cell by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell.

With regard to claim 18, the scope and content of the prior art includes, in the Horch et al. disclosure, a description of a memory cell, comprising an access transistor 350 or 360 on a semiconductor-on-insulator (note figures 1 and 2) substrate, the access transistor 350 or 360 having a floating body (part of second diffusion 2) and a first diffusion region 356 (fig. 3) or 364 (fig. 9) connected to a bit line 430 or 435 and a second diffusion region 354 (fig. 3) or 356 (fig. 9), the second diffusion region 354 (fig. 3) or 356 (fig. 9) to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) thyristor including junction diode 330 or 930 connected between the second diffusion region 354 (fig. 3) or 356 (fig. 9) of the access transistor 350 or 360 and a diode reference potential line 440 (see fig. 4), the diode 330 or 930 having an anode 332 or 932 and a cathode 338 or 938, the diode 330 or 930 being vertically oriented over the access transistor 350 or 360, said cell being reasonable capable, should circumstances arise, of performing the function of enhancing diode 330 or 930 switching with intentionally-generated charges in the floating body of the access transistor 350 or 360. Note figures 1-4,9, column 6 lines 42-67, column 7, column 8 lines 31-67, and column 10 lines 39-67 of Horch et al. Note, column 11 lines 41-57, that Horch et al. did not explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. "[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art

Art Unit: 2826

would employ.” CATAN, 83 USPQ2d at 1573, quoting KSR, 127 S.Ct. at 1741, 82 USPQ2d at 1396.

The difference between the prior art memory cell disclosed by Horch et al. and the claimed device is that, where the claim(s) requires an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode, Horch et al.’s memory cell includes an N-P-N-P negative resistance thyristor. However, Baba discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Baba. The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claim 18 by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for Horch et al.’s N-P-N-P negative resistance thyristor?

To base a claim rejection on the framework of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

- (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;
- (2) a finding that the substituted components and their functions were known in the art;
- (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and
- (4) whatever additional findings based on the Graham factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Horch et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode) for other components (a N-P-N-P negative resistance thyristor). Baba discloses that the substituted components and their functions were known in the art. Further, Baba discloses that those of skill in the art were familiar with a method of combining the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode with a memory cell very

Art Unit: 2826

similar to Horch et al.'s memory cell. From the similarities between the I/V response curves of Baba's P-I-N negative resistance diode and the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell, one of skill in the art would have been able to conclude that Baba's P-I-N negative resistance diode would have been substitutable for the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell) that Baba's P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Horch et al.'s memory cell, and that in said combination Horch et al.'s memory cell would continue functioning in the manner disclosed by Horch et al. It would therefore have been obvious to a person having skill in the art to modify Horch et al.'s memory cell by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell.

With regard to claim 19, the scope and content of the prior art includes, in the Horch et al. disclosure, a description of a memory cell, comprising an access transistor 350 or 360 on a semiconductor-on-insulator (note figures 1 and 2) substrate, the access transistor 350 or 360 having a floating body (part of second diffusion 2) and a first diffusion region 356 (fig. 3) or 364 (fig. 9) connected to a bit line 430 or 435 and a second diffusion region 354 (fig. 3) or 356 (fig. 9), the second diffusion region 354 (fig. 3) or 356 (fig. 9) to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) thyristor including junction diode 330 or 930 connected between the second diffusion region 354 (fig. 3) or 356 (fig. 9) of the access transistor 350 or 360 and a diode reference potential line 440 (see fig. 4), the diode 330 or 930 having an anode 332 or 932 and a cathode 338 or 938, the diode 330 or 930 being vertically oriented over the access transistor 350 or 360, said cell being reasonable capable, should circumstances arise, of performing the function of enhancing diode 330 or 930 switching with intentionally-generated charges in the floating body of the access transistor 350 or 360. Note figures 1-4,9, column 6 lines 42-67, column 7, column 8 lines 31-67, and column 10 lines 39-67 of Horch et al. Note, column 11 lines 41-57, that Horch et

Art Unit: 2826

al. did not explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. “[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.” CATAN, 83 USPQ2d at 1573, quoting KSR, 127 S.Ct. at 1741, 82 USPQ2d at 1396.

The difference between the prior art memory cell disclosed by Horch et al. and the claimed device is that, where the claim(s) requires an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode, Horch et al.’s memory cell includes an N-P-N-P negative resistance thyristor. However, Baba discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Baba. The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claim 19 by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for Horch et al.’s N-P-N-P negative resistance thyristor?

To base a claim rejection on the framework of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

- (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;
- (2) a finding that the substituted components and their functions were known in the art;
- (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and
- (4) whatever additional findings based on the Graham factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Horch et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (an NDR diode

including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode) for other components (a N-P-N-P negative resistance thyristor). Baba discloses that the substituted components and their functions were known in the art. Further, Baba discloses that those of skill in the art were familiar with a method of combining the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode with a memory cell very similar to Horch et al.'s memory cell. From the similarities between the I/V response curves of Baba's P-I-N negative resistance diode and the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell, one of skill in the art would have been able to conclude that Baba's P-I-N negative resistance diode would have been substitutable for the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell) that Baba's P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Horch et al.'s memory cell, and that in said combination Horch et al.'s memory cell would continue functioning in the manner disclosed by Horch et al. It would therefore have been obvious to a person having skill in the art to modify Horch et al.'s memory cell by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell.

With regard to claims 20-28, 30, and 31, the scope and content of the prior art includes, in the Horch et al. disclosure, a description of a memory cell, comprising an access transistor 350 or 360, including a body region 355 or 365; a first diffusion region 356 (fig. 3) or 364 (fig. 9) electrically connected to a bit line 430 or 435; a second diffusion region 354 (fig. 3) or 356 (fig. 9) separated from the first diffusion region 356 (fig. 3) or 364 (fig. 9) by a channel area in the body region 355 or 365; a gate (seen attached to word line 424 or 484) separated from the channel area by a gate insulator (seen between the gate and body region 355 or 365), the gate electrically connected to a word line 424 or 484; a Negative Differential Resistance (NDR) thyristor including junction diode 330 or 930, including an anode 332 or 932 and a cathode 338 or 938, the diode

330 or 930 being connected between the second diffusion region 354 (fig. 3) or 356 (fig. 9) and a diode reference potential line 440 (see fig. 4), said cell being reasonable capable, should circumstances arise, of performing the function of operating to store and sense a charge in the second diffusion region 354 (fig. 3) or 356 (fig. 9) that may be representative of a memory state, wherein the access transistor 350 or 360 may include an n-channel transistor or a p-channel transistor, wherein the diode 330 or 930 may include a p/n diode 330 or 930 having a p-type anode 332 or 932 and an n-type cathode 338 or 938, the p/n diode 330 or 930 may include a p+/n+ diode 330 or 930 having a p+ anode 332 or 932 and an n+ cathode 338 or 938, the diode 330 or 930 may include an n/p diode 330 or 930 having an n-type anode 332 or 932 and a p-type cathode 338 or 938, or an n+/p diode 330 or 930 having an n+ anode 332 or 932 and a p cathode 338 or 938, wherein the diode 330 or 930 may include a laterally-oriented or vertically-oriented diode 330 or 930 or a gate-controlled N-P-N-P thyristor 330 or 930 to enhance switching performance and reduce standby power, and the access transistor 350 or 360 may be on a semiconductor-on-insulator (note figures 1 and 2) or bulk semiconductor (note figures 3 and 9) substrate. Note figures 1-4,9, column 6 lines 42-67, column 7, column 8 lines 31-67, and column 10 lines 39-67 of Horch et al. Note, column 11 lines 41-57, that Horch et al. did not explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. "[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." CATAN, 83 USPQ2d at 1573, quoting KSR, 127 S.Ct. at 1741, 82 USPQ2d at 1396.

The difference between the prior art memory cell disclosed by Horch et al. and the device of claims 20-28, 30, and 31 is that, where the claim(s) requires an NDR diode including an intrinsic region between the anode and the cathode, Horch et al.'s memory cell includes an N-P-N-P negative resistance thyristor. However, Baba discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Baba.

Art Unit: 2826

The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claims 20-28, 30, and 31 by substituting the NDR diode including an intrinsic region between the anode and the cathode taught by Baba for Horch et al.'s N-P-N-P negative resistance thyristor?

To base a claim rejection on the framework of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

- (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;
- (2) a finding that the substituted components and their functions were known in the art;
- (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and
- (4) whatever additional findings based on the Graham factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Horch et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (a NDR diode including an intrinsic region between the anode and the cathode) for other components (a N-P-N-P negative resistance thyristor). Baba discloses that the substituted components and their functions were known in the art. Further, Baba discloses that those of skill in the art were familiar with a method of combining a NDR diode including an intrinsic region between the anode and the cathode with a memory cell very similar to Horch et al.'s memory cell. From the similarities between the I/V response curves of Baba's P-I-N negative resistance diode and the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell, one of skill in the art would have been able to conclude that Baba's P-I-N negative resistance diode would have been substitutable for the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell) that Baba's P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Horch et al.'s memory cell, and that in said combination Horch et al.'s memory cell would continue functioning in the manner disclosed by Horch et al. It would

Art Unit: 2826

therefore have been obvious to a person having skill in the art to modify Horch et al.'s memory cell by substituting the NDR diode including an intrinsic region between the anode and the cathode taught by Baba for the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell.

With regard to claim 29, the scope and content of the prior art includes, in the Horch et al. disclosure, a description of a memory cell, comprising an access transistor 350 or 360, including a body region 355 or 365; a first diffusion region 356 (fig. 3) or 364 (fig. 9) electrically connected to a bit line 430 or 435; a second diffusion region 354 (fig. 3) or 356 (fig. 9) separated from the first diffusion region 356 (fig. 3) or 364 (fig. 9) by a channel area in the body region 355 or 365; a gate (seen attached to word line 424 or 484) separated from the channel area by a gate insulator (seen between the gate and body region 355 or 365), the gate electrically connected to a word line 424 or 484; a Negative Differential Resistance (NDR) thyristor including junction diode 330 or 930, including an anode 332 or 932 and a cathode 338 or 938, the diode 330 or 930 being connected between the second diffusion region 354 (fig. 3) or 356 (fig. 9) and a diode reference potential line 440 (see fig. 4), said cell being reasonable capable, should circumstances arise, of performing the function of operating to store and sense a charge in the second diffusion region 354 (fig. 3) or 356 (fig. 9) that may be representative of a memory state. Note figures 1-4,9, column 6 lines 42-67, column 7, column 8 lines 31-67, and column 10 lines 39-67 of Horch et al. Note, column 11 lines 41-57, that Horch et al. did not explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. "[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." CATAN, 83 USPQ2d at 1573, quoting KSR, 127 S.Ct. at 1741, 82 USPQ2d at 1396.

The difference between the prior art memory cell disclosed by Horch et al. and the claimed device is that, where claim 29 requires an NDR diode formed so as to include an intrinsic region, between the anode and the cathode of the NDR diode, having a de-

Art Unit: 2826

sired geometry to assist with stabilizing the state of the NDR diode, Horch et al.'s memory cell includes an N-P-N-P negative resistance thyristor. However, Baba discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14, having a desired geometry to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Baba. The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claim 29 by substituting the NDR diode formed so as to include an intrinsic region, between the anode and the cathode of the NDR diode, having a desired geometry to assist with stabilizing the state of the NDR diode taught by Baba for Horch et al.'s N-P-N-P negative resistance thyristor?

To base a claim rejection on the framework of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

- (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;
- (2) a finding that the substituted components and their functions were known in the art;
- (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and
- (4) whatever additional findings based on the Graham factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Horch et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (a NDR diode formed so as to include an intrinsic region, between the anode and the cathode of the NDR diode, having a desired geometry to assist with stabilizing the state of the NDR diode) for other components (a N-P-N-P negative resistance thyristor). Baba discloses that the substituted components and their functions were known in the art. Further, Baba discloses that those of skill in the art were familiar with a method of combining the NDR diode formed so as to include an intrinsic region, between the anode and the cathode of the NDR diode, having a desired geometry to assist with stabilizing the state of the NDR diode with a memory cell very similar to Horch et al.'s memory cell. From the similarities between the I/V response curves of Baba's P-I-N negative resistance di-

Art Unit: 2826

ode and the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell, one of skill in the art would have been able to conclude that Baba's P-I-N negative resistance diode would have been substitutable for the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell) that Baba's P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Horch et al.'s memory cell, and that in said combination Horch et al.'s memory cell would continue functioning in the manner disclosed by Horch et al. It would therefore have been obvious to a person having skill in the art to modify Horch et al.'s memory cell by substituting the NDR diode formed so as to include an intrinsic region, between the anode and the cathode of the NDR diode, having a desired geometry to assist with stabilizing the state of the NDR diode taught by Baba for the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell.

With regard to claims 33-41, the scope and content of the prior art includes, in the Horch et al. disclosure, a description of a memory cell, comprising an access transistor 350 or 360 formed in a bulk semiconductor (note figures 3 and 9) structure, the access transistor 350 or 360 including a first diffusion region 356 (fig. 3) or 364 (fig. 9) separated from a second diffusion region 354 (fig. 3) or 356 (fig. 9) by a channel region, and further including a gate (seen attached to word line 424 or 484) separated from the channel region by a gate insulator (seen between the gate and body region 355 or 365), wherein the first diffusion region 356 (fig. 3) or 364 (fig. 9) may be connected to a bit line 430 or 435 and the gate may be connected to a first word line 424 or 484; and a gate-controlled Negative Differential Resistance (NDR) thyristor including junction diode 330 or 930 connected between a reference potential line 440 (see fig. 4) and the second diffusion region 354 (fig. 3) or 356 (fig. 9), the diode 330 or 930 including an anode 332 or 932, a cathode 338 or 938, and a diode gate 313 or 913 connected to a second word line 420 or 480, wherein the gate-controlled N-P-N-P thyristor 330 or 930 may include a laterally-oriented diode 330 or 930 positioned over the access transistor 350 or 360, or a vertically-oriented diode 330 or 930, the first and second diffusion region 354 (fig. 3) or 356 (fig. 9)s of the access transistor 350 or 360 include n-type or p-type dopants; and

Art Unit: 2826

the gate-controlled N-P-N-P thyristor 330 or 930 may include a p/n or n/p diode 330 or 930 having a p-type or n-type anode 332 or 932 connected to the reference potential line 440 (see fig. 4) and an n-type or p-type cathode 338 or 938 formed with the second diffusion region 354 (fig. 3) or 356 (fig. 9). Note figures 1-4,9, column 6 lines 42-67, column 7, column 8 lines 31-67, and column 10 lines 39-67 of Horch et al. Note, column 11 lines 41-57, that Horch et al. did not explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. “[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.” CATAN, 83 USPQ2d at 1573, quoting KSR, 127 S.Ct. at 1741, 82 USPQ2d at 1396.

The applicant's claim 36 does not distinguish over the Horch et al. reference regardless of the process used to form the lateral-orientated diode, because only the final product is relevant, not the recited process of using raised source/drain techniques and metal-induced-lateral crystallization techniques. See *SmithKline Beecham Corp. v. Apotex Corp.*, 78 USPQ2d 1097 (Fed. Cir, 2006 (“While the process set forth in the product-by-process claim may be new, that novelty can only be captured by obtaining a process claim.”))

Note that when “product by process” claiming is used to describe one or more limitations of a claimed product, the limitations so described are limitations of the claimed product per se, no matter how said product is actually made. In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a “product by process” claim and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in “product by process” claims or not. Note that

Art Unit: 2826

applicant has the burden of proof in such cases, as the above caselaw makes clear.

See also MPEP 706.03(e).

The Federal Circuit recently revisited the question of whether a “product by process” claim can be anticipated by a reference that does not recite said process. See *Smith-Kline Beecham Corp. v. Apotex Corp.*, 78 USPQ2d at 1100. The Federal Circuit cited with approval this Office’s current statement of the law, found in MPEP § 2113:

[Even] though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process.

Id. at 1101. The Federal Circuit held this statement to be consistent with its own views on this topic, as well as various Supreme Court rulings, notably *Gen. Elec. Co. v. Wabash Appliance Corp.*, 304 U.S. 364, 373 (1938) (“Although in some instances a claim may validly describe a new product with some reference to the method of production, a patentee who does not distinguish his product from what is old except by reference, express or constructive, to the process by which he produced it, cannot secure a monopoly on the product by whatever means produced.”). *Id.*

The difference between the prior art memory cell disclosed by Horsch et al. and the claimed device is that, where claims 33-41 require an NDR diode formed so as to include an intrinsic region, between the anode and the cathode of the NDR diode, having a desired geometry to assist with stabilizing the state of the NDR diode and operatively positioned to enhance switching performance, Horsch et al.’s memory cell includes an N-P-N-P negative resistance thyristor. However, Baba discloses a P-I-N negative resistance diode 10 formed so as to include an intrinsic region 13, between an anode 11 and a cathode 14 of the diode, having a desired geometry to assist with stabilizing the state of the diode and be operatively positioned to enhance switching performance. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Baba. The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claims 33-41 by substituting the NDR diode formed so as to include an intrinsic region, between the anode and the cathode of the NDR diode, having a desired geometry to assist with sta-

Art Unit: 2826

bilizing the state of the NDR diode and operatively positioned to enhance switching performance taught by Baba for Horch et al.'s N-P-N-P negative resistance thyristor?

To base a claim rejection on the framework of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

- (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;
- (2) a finding that the substituted components and their functions were known in the art;
- (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and
- (4) whatever additional findings based on the Graham factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Horch et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (a NDR diode formed so as to include an intrinsic region, between the anode and the cathode of the NDR diode, having a desired geometry to assist with stabilizing the state of the NDR diode and operatively positioned to enhance switching performance) for other components (a N-P-N-P negative resistance thyristor). Baba discloses that the substituted components and their functions were known in the art. Further, Baba discloses that those of skill in the art were familiar with a method of combining the NDR diode formed so as to include an intrinsic region, between the anode and the cathode of the NDR diode, having a desired geometry to assist with stabilizing the state of the NDR diode and operatively positioned to enhance switching performance with a memory cell very similar to Horch et al.'s memory cell. From the similarities between the I/V response curves of Baba's P-I-N negative resistance diode and the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell, one of skill in the art would have been able to conclude that Baba's P-I-N negative resistance diode would have been substitutable for the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell) that Baba's P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Horch et al.'s memory cell, and that in said combination

Art Unit: 2826

Horch et al.'s memory cell would continue functioning in the manner disclosed by Horch et al. It would therefore have been obvious to a person having skill in the art to modify Horch et al.'s memory cell by substituting the NDR diode formed so as to include an intrinsic region, between the anode and the cathode of the NDR diode, having a desired geometry to assist with stabilizing the state of the NDR diode and operatively positioned to enhance switching performance taught by Baba for the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell.

With regard to claims 42-53, the scope and content of the prior art includes, in the Horch et al. disclosure, a description of a memory cell, comprising an semiconductor-on-insulator (note figures 1 and 2) (SOI) structure, including an SOI access transistor 350 or 360 including a first diffusion region 356 (fig. 3) or 364 (fig. 9) separated from a second diffusion region 354 (fig. 3) or 356 (fig. 9) by a channel region, and further including a gate (seen attached to word line 424 or 484) separated from the channel region by a gate insulator (seen between the gate and body region 355 or 365), wherein the first diffusion region 356 (fig. 3) or 364 (fig. 9) may be connected to a bit line 430 or 435 and the gate may be connected to a first word line 424 or 484; and a Negative Differential Resistance (NDR) thyristor including junction diode 330 or 930 connected between the second diffusion region 354 (fig. 3) or 356 (fig. 9) and a reference potential line 440 (see fig. 4), the diode 330 or 930 including an anode 332 or 932, a cathode 338 or 938, a diode gate 313 or 913 connected to a second word line 420 or 480; the anode 332 or 932 and the cathode 338 or 938 having a desired geometry to store a charge indicative of a memory state and being operably positioned with respect to the diode gate 313 or 913, wherein the diode 330 or 930 may include a lateral-oriented diode 330 or 930 positioned over the access transistor 350 or 360 and the SOI access transistor 350 or 360 and the lateral-oriented diode 330 or 930 may be formed in a semiconductor volume over a buried oxide (BOX) region, the diode 330 or 930 may include a vertical-oriented diode 330 or 930 including the second diffusion region 354 (fig. 3) or 356 (fig. 9) of the access transistor 350 or 360, and the first and second diffusion region 354 (fig. 3) or 356 (fig. 9)s of the access transistor 350 or 360 may include n-type or p-type dopants; and the gate-controlled N-P-N-P thyristor 330 or 930 may include a p/n or n/p diode 330 or 930 having an n-type or p-type anode 332 or 932 connected to the refer-

Art Unit: 2826

ence potential line 440 (see fig. 4) and a p-type or n-type cathode 338 or 938 formed with the second diffusion region 354 (fig. 3) or 356 (fig. 9). Note figures 1-4,9, column 6 lines 42-67, column 7, column 8 lines 31-67, and column 10 lines 39-67 of Horch et al. Note, column 11 lines 41-57, that Horch et al. did not explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. “[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.” CATAN, 83 USPQ2d at 1573, quoting KSR, 127 S.Ct. at 1741, 82 USPQ2d at 1396.

The applicant's claim 46 does not distinguish over the Horch et al. reference regardless of the process used to form the lateral-orientated diode, because only the final product is relevant, not the recited process of using raised source/drain techniques and metal-induced-lateral crystallization techniques. See *SmithKline Beecham Corp. v. Apotex Corp.*, 78 USPQ2d 1097 (Fed. Cir, 2006 (“While the process set forth in the product-by-process claim may be new, that novelty can only be captured by obtaining a process claim.”))

The difference between the prior art memory cell disclosed by Horch et al. and the device of claims 42-53 is that, where the claim(s) requires an NDR diode including an intrinsic region between the anode and the cathode, Horch et al.'s memory cell includes an N-P-N-P negative resistance thyristor. However, Baba discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Baba. The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claims 42-53 by substituting the NDR diode including an intrinsic region between the anode and the cathode taught by Baba for Horch et al.'s N-P-N-P negative resistance thyristor?

Art Unit: 2826

To base a claim rejection on the framework of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

- (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;
- (2) a finding that the substituted components and their functions were known in the art;
- (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and
- (4) whatever additional findings based on the Graham factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Horch et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (a NDR diode including an intrinsic region between the anode and the cathode) for other components (a N-P-N-P negative resistance thyristor). Baba discloses that the substituted components and their functions were known in the art. Further, Baba discloses that those of skill in the art were familiar with a method of combining a NDR diode including an intrinsic region between the anode and the cathode with a memory cell very similar to Horch et al.'s memory cell. From the similarities between the I/V response curves of Baba's P-I-N negative resistance diode and the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell, one of skill in the art would have been able to conclude that Baba's P-I-N negative resistance diode would have been substitutable for the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell) that Baba's P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Horch et al.'s memory cell, and that in said combination Horch et al.'s memory cell would continue functioning in the manner disclosed by Horch et al. It would therefore have been obvious to a person having skill in the art to modify Horch et al.'s memory cell by substituting the NDR diode including an intrinsic region between the anode and the cathode taught by Baba for the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell.

Art Unit: 2826

With regard to claims 54-62, the scope and content of the prior art includes, in the Horch et al. disclosure, a description of a memory cell, comprising an access transistor 350 or 360, the access transistor 350 or 360 including a first diffusion region 356 (fig. 3) or 364 (fig. 9) separated from a second diffusion region 354 (fig. 3) or 356 (fig. 9) by a channel region, and further including a gate (seen attached to word line 424 or 484) separated from the channel region by a gate insulator (seen between the gate and body region 355 or 365), wherein the first diffusion region 356 (fig. 3) or 364 (fig. 9) may be connected to a bit line 430 or 435 and the gate may be connected to a first word line 424 or 484; and a Negative Differential Resistance (NDR) p+/n+ diode 330 or 930 connected between a diode reference potential line 440 (see fig. 4) and the second diffusion region 354 (fig. 3) or 356 (fig. 9), the p/n diode 330 or 930 including a p+ anode 332 or 932, an n+ cathode 338 or 938, and a diode gate 313 or 913 connected to a second word line 420 or 480, wherein the diode 330 or 930 may include a laterally-oriented or vertically-oriented diode 330 or 930 or a gate-controlled N-P-N-P thyristor 330 or 930 to enhance switching performance and reduce standby power, and the access transistor 350 or 360 may include a p-channel or n-channel transistor on a semiconductor-on-insulator (note figures 1 and 2) or bulk semiconductor (note figures 3 and 9) substrate. Note figures 1-4,9, column 6 lines 42-67, column 7, column 8 lines 31-67, and column 10 lines 39-67 of Horch et al. Note, column 11 lines 41-57, that Horch et al. did not explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. "[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." CATAN, 83 USPQ2d at 1573, quoting KSR, 127 S.Ct. at 1741, 82 USPQ2d at 1396.

The difference between the prior art memory cell disclosed by Horch et al. and the claimed device is that, where claims 54-62 require an NDR diode including an intrinsic region operably positioned between an anode and a cathode, Horch et al.'s memory cell includes an N-P-N-P negative resistance thyristor. However, Baba discloses a P-I-N

Art Unit: 2826

negative resistance diode 10 with an intrinsic region 13 operably positioned between an anode 11 and a cathode 14. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Baba. The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claims 54-62 by substituting the NDR diode including an intrinsic region operably positioned between an anode and a cathode taught by Baba for Horch et al.'s N-P-N-P negative resistance thyristor?

To base a claim rejection on the framework of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

- (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;
- (2) a finding that the substituted components and their functions were known in the art;
- (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and
- (4) whatever additional findings based on the Graham factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Horch et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (a NDR diode including an intrinsic region operably positioned between an anode and a cathode) for other components (a N-P-N-P negative resistance thyristor). Baba discloses that the substituted components and their functions were known in the art. Further, Baba discloses that those of skill in the art were familiar with a method of combining the NDR diode including an intrinsic region operably positioned between an anode and a cathode with a memory cell very similar to Horch et al.'s memory cell. From the similarities between the I/V response curves of Baba's P-I-N negative resistance diode and the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell, one of skill in the art would have been able to conclude that Baba's P-I-N negative resistance diode would have been substitutable for the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell) that Baba's P-I-N negative resistance diode would have con-

Art Unit: 2826

tinued functioning much as it did before being substituted into Horch et al.'s memory cell, and that in said combination Horch et al.'s memory cell would continue functioning in the manner disclosed by Horch et al. It would therefore have been obvious to a person having skill in the art to modify Horch et al.'s memory cell by substituting the NDR diode including an intrinsic region operably positioned between an anode and a cathode taught by Baba for the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell.

With regard to claims 63-71, the scope and content of the prior art includes, in the Horch et al. disclosure, a description of a memory cell, comprising an access transistor 350 or 360, the access transistor 350 or 360 including a first diffusion region 356 (fig. 3) or 364 (fig. 9) separated from a second diffusion region 354 (fig. 3) or 356 (fig. 9) by a channel region, and further including a gate (seen attached to word line 424 or 484) separated from the channel region by a gate insulator (seen between the gate and body region 355 or 365), wherein the first diffusion region 356 (fig. 3) or 364 (fig. 9) may be connected to a bit line 430 or 435 and the gate may be connected to a first word line 424 or 484; and a Negative Differential Resistance (NDR) n+/p diode 330 or 930 connected between a diode reference potential line 440 (see fig. 4) and the second diffusion region 354 (fig. 3) or 356 (fig. 9), the p/n diode 330 or 930 including an n+ anode 332 or 932, a p cathode 338 or 938, and a diode gate 313 or 913 connected to a second word line 420 or 480, wherein the diode 330 or 930 may include a laterally-oriented or vertically-oriented diode 330 or 930 or a gate-controlled N-P-N-P thyristor 330 or 930 to enhance switching performance and reduce standby power, and the access transistor 350 or 360 may include a p-channel or n-channel transistor on a semiconductor-on-insulator (note figures 1 and 2) or bulk semiconductor (note figures 3 and 9) substrate. Note figures 1-4,9, column 6 lines 42-67, column 7, column 8 lines 31-67, and column 10 lines 39-67 of Horch et al. Note, column 11 lines 41-57, that Horch et al. did not explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. "[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take ac-

Art Unit: 2826

count of the inferences and creative steps that a person of ordinary skill in the art would employ.” CATAN, 83 USPQ2d at 1573, quoting KSR, 127 S.Ct. at 1741, 82 USPQ2d at 1396.

The difference between the prior art memory cell disclosed by Horch et al. and the claimed device is that, where claims 63-71 require an NDR diode including an intrinsic region operably positioned between an anode and a cathode, Horch et al.’s memory cell includes an N-P-N-P negative resistance thyristor. However, Baba discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 operably positioned between an anode 11 and a cathode 14. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Baba. The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claims 63-71 by substituting the NDR diode including an intrinsic region operably positioned between an anode and a cathode taught by Baba for Horch et al.’s N-P-N-P negative resistance thyristor?

To base a claim rejection on the framework of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

- (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;
- (2) a finding that the substituted components and their functions were known in the art;
- (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and
- (4) whatever additional findings based on the Graham factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Horch et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (a NDR diode including an intrinsic region operably positioned between an anode and a cathode) for other components (a N-P-N-P negative resistance thyristor). Baba discloses that the substituted components and their functions were known in the art. Further, Baba discloses that those of skill in the art were familiar with a method of combining the NDR diode including an intrinsic region operably positioned between an anode and a cathode with a memory cell very similar to Horch et al.’s memory cell. From the similarities be-

Art Unit: 2826

tween the I/V response curves of Baba's P-I-N negative resistance diode and the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell, one of skill in the art would have been able to conclude that Baba's P-I-N negative resistance diode would have been substitutable for the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell) that Baba's P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Horch et al.'s memory cell, and that in said combination Horch et al.'s memory cell would continue functioning in the manner disclosed by Horch et al. It would therefore have been obvious to a person having skill in the art to modify Horch et al.'s memory cell by substituting the NDR diode including an intrinsic region operably positioned between an anode and a cathode taught by Baba for the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell.

With regard to claims 72-79, the scope and content of the prior art includes, in the Horch et al. disclosure, a description of a memory device, comprising a memory array, including a plurality of memory cells in rows and columns; a number of word lines 424 and 484, each word line 424 or 484 connected to a row of memory cells; a number of bit lines 430 and 435, each bit line 430 or 435 connected to a column of memory cells; at least one reference line 440 to provide a reference potential to the memory cells; control circuitry, including word line 424 or 484, select circuitry and bit line select circuitry to select a number of memory cells for writing and reading operations, wherein each memory cell may include an access transistor 350 or 360, including a body region 355 or 365, a first diffusion region 356 (fig. 3) or 364 (fig. 9) electrically connected to one of the bit lines 430 and 435, a second diffusion region 354 (fig. 3) or 356 (fig. 9) separated from the first diffusion region 356 (fig. 3) or 364 (fig. 9) by a channel area in the body region 355 or 365, and a gate (seen attached to word line 424 or 484) separated from the channel area by a gate insulator (seen between the gate and body region 355 or 365) and electrically connected to one of the word lines 424 and 484; and a Negative Differential Resistance (NDR) gate-controlled N-P-N-P thyristor 330 or 930, including an anode 332 or 932 and a cathode 338 or 938, the diode 330 or 930 being connected be-

tween the second diffusion region 354 (fig. 3) or 356 (fig. 9) and a diode 330 or 930 reference line, wherein the memory cell may be adapted to store a charge in the second diffusion region 354 (fig. 3) or 356 (fig. 9) of the access transistor 350 or 360 to indicate a stable memory state, wherein each memory cell may be on a bulk semiconductor (note figures 3 and 9) substrate, and the diode 330 or 930 may include a vertically-oriented diode 330 or 930 or a laterally-oriented diode 330 or 930 over the access transistor 350 or 360, or each memory cell may be on a semiconductor-on-insulator (note figures 1 and 2) substrate such that the access transistor 350 or 360 has a floating body (part of second diffusion 2), and the diode 330 or 930 may include a laterally-oriented diode 330 or 930 formed over, or at least partially in the floating body of, the access transistor 350 or 360. Note figures 1-4,9, column 6 lines 42-67, column 7, column 8 lines 31-67, and column 10 lines 39-67 of Horch et al. Note, column 11 lines 41-57, that Horch et al. did not explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. "[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." CATAN, 83 USPQ2d at 1573, quoting KSR, 127 S.Ct. at 1741, 82 USPQ2d at 1396.

The difference between the prior art memory cell disclosed by Horch et al. and the claimed device is that, where claims 72-79 require an NDR diode including an intrinsic region between an anode and a cathode, Horch et al.'s memory cell includes an N-P-N-P negative resistance thyristor. However, Baba discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Baba. The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claims 72-79 by substituting the NDR diode including an intrinsic region between an anode and a cathode taught by Baba for Horch et al.'s N-P-N-P negative resistance thyristor?

Art Unit: 2826

To base a claim rejection on the framework of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

- (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;
- (2) a finding that the substituted components and their functions were known in the art;
- (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and
- (4) whatever additional findings based on the Graham factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Horch et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (a NDR diode including an intrinsic region between an anode and a cathode) for other components (a N-P-N-P negative resistance thyristor). Baba discloses that the substituted components and their functions were known in the art. Further, Baba discloses that those of skill in the art were familiar with a method of combining the NDR diode including an intrinsic region between an anode and a cathode with a memory cell very similar to Horch et al.'s memory cell. From the similarities between the I/V response curves of Baba's P-I-N negative resistance diode and the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell, one of skill in the art would have been able to conclude that Baba's P-I-N negative resistance diode would have been substitutable for the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell) that Baba's P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Horch et al.'s memory cell, and that in said combination Horch et al.'s memory cell would continue functioning in the manner disclosed by Horch et al. It would therefore have been obvious to a person having skill in the art to modify Horch et al.'s memory cell by substituting the NDR diode including an intrinsic region between an anode and a cathode taught by Baba for the N-P-N-P negative resistance thyristor of Horch et al.'s memory cell.

Art Unit: 2826

B. Applicants will be aware that, date-wise, Horch et al. does not present an insurmountable bar to the patentability of their claims. In the interests of compact prosecution, therefore, claims 1-79 are rejected under 35 U.S.C. 103(a) as being unpatentable over NEMATI ET AL. (6,229,161) (published 5/8/2001) in view of BABA (5,686,739). In the examiner's opinion, this/these claim(s) would have been obvious according to one of the rationales expressed in the *Examination Guidelines for Determining Obviousness Under 35 U.S.C. 103 in View of the Supreme Court Decision in KSR International Co. v. Teleflex Inc.*, as published at 72 Federal Register 57526 et seq. (10/10/2007).

We begin by considering the first and second factual findings (factual findings concerning the level of skill in the art are laid out above. The level of skill in the semiconductor art is a level of creativity, scientific thinking, and applied problem-solving unprecedented in the history of Man) required by Graham. With regard to claims 1-5, the scope and content of the prior art includes, in the Nemati et al. disclosure, a description of a memory cell, comprising an access transistor 12 having a floating node 24, the floating node 24 to store a charge indicative of a memory state of the memory cell; and a gate-controlled diode 10 exhibiting Negative Differential Resistance (NDR) behavior connected between the floating node 24 and a diode reference potential line 19, the diode 10 including an anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19) and a cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24), wherein the cathode of the diode 10 may be connected to the floating node 24 of the access transistor 12 and the access transistor 12 may be formed in either a bulk semiconductor (note figure 6) structure or a semiconductor-on-insulator (note figure 6a) structure. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al. Note, column 7 lines 16-31, that Nemati et al. did not explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. "[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the

Art Unit: 2826

inferences and creative steps that a person of ordinary skill in the art would employ.”

CATAN, 83 USPQ2d at 1573, quoting KSR, 127 S.Ct. at 1741, 82 USPQ2d at 1396.

The difference between the prior art memory cell disclosed by Nemati et al. and the claimed device is that, where the claim(s) requires an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode, Nemati et al.’s memory cell includes an N-P-N-P negative resistance thyristor. However, Baba discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Baba. The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claims 1-5 by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for Nemati et al.’s N-P-N-P negative resistance thyristor?

To base a claim rejection on the framework of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

- (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;
- (2) a finding that the substituted components and their functions were known in the art;
- (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and
- (4) whatever additional findings based on the Graham factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Nemati et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode) for other components (a N-P-N-P negative resistance thyristor). Baba discloses that the substituted components and their functions were known in the art. Further, Baba discloses that those of skill in the art were familiar with a method of combining the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode with a memory cell very

similar to Nemati et al.'s memory cell. From the similarities between the I/V response curves of Baba's P-I-N negative resistance diode and the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell, one of skill in the art would have been able to conclude that Baba's P-I-N negative resistance diode would have been substitutable for the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell) that Baba's P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Nemati et al.'s memory cell, and that in said combination Nemati et al.'s memory cell would continue functioning in the manner disclosed by Nemati et al. It would therefore have been obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell.

With regard to claim 6, the scope and content of the prior art includes, in the Nemati et al. disclosure, a description of a memory cell, comprising an access transistor 12 having a first diffusion region (not numbered; seen directly under bit line 18) connected to a bit line 18, and a second diffusion region 24, the second diffusion region 24 to store a charge indicative of a memory state of the memory cell; a Negative Differential Resistance (NDR) diode 10 connected between the second diffusion region 24 and a diode reference potential line 19, the diode 10 including an anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19); a cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24); and a diode gate 20. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al. Note, column 7 lines 16-31, that Nemati et al. did not explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. "[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged

Art Unit: 2826

claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.” CATAN, 83 USPQ2d at 1573, quoting KSR, 127 S.Ct. at 1741, 82 USPQ2d at 1396.

The difference between the prior art memory cell disclosed by Nemati et al. and the claimed device is that, where the claim(s) requires an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode, and operatively positioned to enhance switching performance, Nemati et al.’s memory cell includes an N-P-N-P negative resistance thyristor. However, Baba discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode, and operatively positioned to enhance switching performance. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Baba. The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claim(s) 6 by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode, and operatively positioned to enhance switching performance taught by Baba for Nemati et al.’s N-P-N-P negative resistance thyristor?

To base a claim rejection on the framework of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

- (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;
- (2) a finding that the substituted components and their functions were known in the art;
- (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and
- (4) whatever additional findings based on the Graham factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Nemati et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (a NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode, and operatively positioned to enhance switching perform-

ance) for other components (a N-P-N-P negative resistance thyristor). Baba discloses that the substituted components and their functions were known in the art. Further, Baba discloses that those of skill in the art were familiar with a method of combining the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode, and operatively positioned to enhance switching performance with a memory cell very similar to Nemati et al.'s memory cell. From the similarities between the I/V response curves of Baba's P-I-N negative resistance diode and the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell, one of skill in the art would have been able to conclude that Baba's P-I-N negative resistance diode would have been substitutable for the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell) that Baba's P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Nemati et al.'s memory cell, and that in said combination Nemati et al.'s memory cell would continue functioning in the manner disclosed by Nemati et al. It would therefore have been obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the P-I-N negative resistance diode taught by Baba for the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell.

With regard to claim 7, the scope and content of the prior art includes, in the Nemati et al. disclosure, a description of a memory cell, comprising an n-channel access transistor 12 on a bulk semiconductor (note figure 6) substrate, the n-channel access transistor 12 having a n-type first diffusion region (not numbered; seen directly under bit line 18) connected to a bit line 18 and an n-type second diffusion region 24, the n-type second diffusion region 24 to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) n/p diode 10 having an n-type anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19) connected to a diode reference potential line 19 and a p-type cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24) in contact with the n-type second diffusion region 24. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al.

Art Unit: 2826

Note, column 7 lines 16-31, that Nemati et al. did not explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. “[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.” CATAN, 83 USPQ2d at 1573, quoting KSR, 127 S.Ct. at 1741, 82 USPQ2d at 1396.

The difference between the prior art memory cell disclosed by Nemati et al. and the claimed device is that, where the claim(s) requires an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode, Nemati et al.’s memory cell includes an N-P-N-P negative resistance thyristor. However, Baba discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Baba. The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claim 7 by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for Nemati et al.’s N-P-N-P negative resistance thyristor?

To base a claim rejection on the framework of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

- (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;
- (2) a finding that the substituted components and their functions were known in the art;
- (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and
- (4) whatever additional findings based on the Graham factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Nemati et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (an NDR diode

including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode) for other components (a N-P-N-P negative resistance thyristor). Baba discloses that the substituted components and their functions were known in the art. Further, Baba discloses that those of skill in the art were familiar with a method of combining the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode with a memory cell very similar to Nemati et al.'s memory cell. From the similarities between the I/V response curves of Baba's P-I-N negative resistance diode and the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell, one of skill in the art would have been able to conclude that Baba's P-I-N negative resistance diode would have been substitutable for the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell) that Baba's P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Nemati et al.'s memory cell, and that in said combination Nemati et al.'s memory cell would continue functioning in the manner disclosed by Nemati et al. It would therefore have been obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell.

With regard to claim 8, the scope and content of the prior art includes, in the Nemati et al. disclosure, a description of a memory cell, comprising a p-channel access transistor 12 on a bulk semiconductor (note figure 6) substrate, the p-channel access transistor 12 having a p-type first diffusion region (not numbered; seen directly under bit line 18) connected to a bit line 18 and a p-type second diffusion region 24, the p-type second diffusion region 24 to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) n/p diode 10 having an n-type anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19) connected to a diode reference potential line 19 and a p-type cathode (part of diode 10 that is adjacent to and sometimes contiguous

Art Unit: 2826

with node 24) formed with the n-type second diffusion region 24. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al. Note, column 7 lines 16-31, that Nemati et al. did not explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. “[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.” CATAN, 83 USPQ2d at 1573, quoting KSR, 127 S.Ct. at 1741, 82 USPQ2d at 1396.

The difference between the prior art memory cell disclosed by Nemati et al. and the claimed device is that, where the claim(s) requires an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode, Nemati et al.’s memory cell includes an N-P-N-P negative resistance thyristor. However, Baba discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Baba. The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claim 8 by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for Nemati et al.’s N-P-N-P negative resistance thyristor?

To base a claim rejection on the framework of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

- (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;
- (2) a finding that the substituted components and their functions were known in the art;
- (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and
- (4) whatever additional findings based on the Graham factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

Art Unit: 2826

As explained above, Nemati et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode) for other components (a N-P-N-P negative resistance thyristor). Baba discloses that the substituted components and their functions were known in the art. Further, Baba discloses that those of skill in the art were familiar with a method of combining the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode with a memory cell very similar to Nemati et al.'s memory cell. From the similarities between the I/V response curves of Baba's P-I-N negative resistance diode and the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell, one of skill in the art would have been able to conclude that Baba's P-I-N negative resistance diode would have been substitutable for the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell) that Baba's P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Nemati et al.'s memory cell, and that in said combination Nemati et al.'s memory cell would continue functioning in the manner disclosed by Nemati et al. It would therefore have been obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell.

With regard to claim 9, the scope and content of the prior art includes, in the Nemati et al. disclosure, a description of a memory cell, comprising an n-channel access transistor 12 on a bulk semiconductor (note figure 6) substrate, the p-channel access transistor 12 having a n-type first diffusion region (not numbered; seen directly under bit line 18) connected to a bit line 18 and an n-type second diffusion region 24, the n-type second diffusion region 24 to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) p/n diode 10 having a p-type anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode

Art Unit: 2826

10 that is adjacent to reference line 19) connected to a diode reference potential line 19 and an n-type cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24) formed with the n-type second diffusion region 24. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al. Note, column 7 lines 16-31, that Nemati et al. did not explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. “[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.” CATAN, 83 USPQ2d at 1573, quoting KSR, 127 S.Ct. at 1741, 82 USPQ2d at 1396.

The difference between the prior art memory cell disclosed by Nemati et al. and the claimed device is that, where the claim(s) requires an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode, Nemati et al.’s memory cell includes an N-P-N-P negative resistance thyristor. However, Baba discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Baba. The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claim 9 by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for Nemati et al.’s N-P-N-P negative resistance thyristor?

To base a claim rejection on the framework of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

- (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;
- (2) a finding that the substituted components and their functions were known in the art;
- (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and

Art Unit: 2826

(4) whatever additional findings based on the Graham factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Nemati et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode) for other components (a N-P-N-P negative resistance thyristor). Baba discloses that the substituted components and their functions were known in the art. Further, Baba discloses that those of skill in the art were familiar with a method of combining the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode with a memory cell very similar to Nemati et al.'s memory cell. From the similarities between the I/V response curves of Baba's P-I-N negative resistance diode and the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell, one of skill in the art would have been able to conclude that Baba's P-I-N negative resistance diode would have been substitutable for the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell) that Baba's P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Nemati et al.'s memory cell, and that in said combination Nemati et al.'s memory cell would continue functioning in the manner disclosed by Nemati et al. It would therefore have been obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell.

With regard to claim 10, the scope and content of the prior art includes, in the Nemati et al. disclosure, a description of a memory cell, comprising a p-channel access transistor 12 on a bulk semiconductor (note figure 6) substrate, the p-channel access transistor 12 having a p-type first diffusion region (not numbered; seen directly under bit line 18) connected to a bit line 18 and a p-type second diffusion region 24, the p-type second diffusion region 24 to store a charge indicative of a memory state of the memory

Art Unit: 2826

cell; and a Negative Differential Resistance (NDR) p/n diode 10 having a p-type anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19) connected to a diode reference potential line 19 and an n-type cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24) in contact with the p-type second diffusion region 24. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al. Note, column 7 lines 16-31, that Nemati et al. did not explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. “[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.” CATAN, 83 USPQ2d at 1573, quoting KSR, 127 S.Ct. at 1741, 82 USPQ2d at 1396.

The difference between the prior art memory cell disclosed by Nemati et al. and the claimed device is that, where the claim(s) requires an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode, Nemati et al.’s memory cell includes an N-P-N-P negative resistance thyristor. However, Baba discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Baba. The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claim 10 by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for Nemati et al.’s N-P-N-P negative resistance thyristor?

To base a claim rejection on the framework of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

- (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;

Art Unit: 2826

- (2) a finding that the substituted components and their functions were known in the art;
- (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and
- (4) whatever additional findings based on the Graham factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Nemati et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode) for other components (a N-P-N-P negative resistance thyristor). Baba discloses that the substituted components and their functions were known in the art. Further, Baba discloses that those of skill in the art were familiar with a method of combining the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode with a memory cell very similar to Nemati et al.'s memory cell. From the similarities between the I/V response curves of Baba's P-I-N negative resistance diode and the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell, one of skill in the art would have been able to conclude that Baba's P-I-N negative resistance diode would have been substitutable for the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell) that Baba's P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Nemati et al.'s memory cell, and that in said combination Nemati et al.'s memory cell would continue functioning in the manner disclosed by Nemati et al. It would therefore have been obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell.

With regard to claim 11, the scope and content of the prior art includes, in the Nemati et al. disclosure, a description of a memory cell, comprising an access transistor 12 on a bulk semiconductor (note figure 6) substrate, the access transistor 12 having a first diffusion region (not numbered; seen directly under bit line 18) connected to a bit

Art Unit: 2826

line 18 and a second diffusion region 24, the second diffusion region 24 to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) diode 10 connected between the second diffusion region 24 of the access transistor 12 and a diode reference potential line 19, the diode 10 having an anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19) and a cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24), the diode 10 being laterally oriented over the access transistor 12. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al. Note, column 7 lines 16-31, that Nemati et al. did not explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. “[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.” CATAN, 83 USPQ2d at 1573, quoting KSR, 127 S.Ct. at 1741, 82 USPQ2d at 1396.

The difference between the prior art memory cell disclosed by Nemati et al. and the claimed device is that, where the claim(s) requires an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode, Nemati et al.’s memory cell includes an N-P-N-P negative resistance thyristor. However, Baba discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Baba. The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claim 11 by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for Nemati et al.’s N-P-N-P negative resistance thyristor?

Art Unit: 2826

To base a claim rejection on the framework of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

- (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;
- (2) a finding that the substituted components and their functions were known in the art;
- (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and
- (4) whatever additional findings based on the Graham factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Nemati et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode) for other components (a N-P-N-P negative resistance thyristor). Baba discloses that the substituted components and their functions were known in the art. Further, Baba discloses that those of skill in the art were familiar with a method of combining the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode with a memory cell very similar to Nemati et al.'s memory cell. From the similarities between the I/V response curves of Baba's P-I-N negative resistance diode and the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell, one of skill in the art would have been able to conclude that Baba's P-I-N negative resistance diode would have been substitutable for the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell) that Baba's P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Nemati et al.'s memory cell, and that in said combination Nemati et al.'s memory cell would continue functioning in the manner disclosed by Nemati et al. It would therefore have been obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the

Art Unit: 2826

NDR diode taught by Baba for the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell.

With regard to claim 12, the scope and content of the prior art includes, in the Nemati et al. disclosure, a description of a memory cell, comprising an access transistor 12 on a bulk semiconductor (note figure 6) substrate, the access transistor 12 having a first diffusion region (not numbered; seen directly under bit line 18) connected to a bit line 18 and a second diffusion region 24, the second diffusion region 24 to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) diode 10 connected between the second diffusion region 24 of the access transistor 12 and a diode reference potential line 19, the diode 10 having an anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19) and a cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24), the diode 10 being vertically oriented over the access transistor 12. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al. Note, column 7 lines 16-31, that Nemati et al. did not explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. "[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." CATAN, 83 USPQ2d at 1573, quoting KSR, 127 S.Ct. at 1741, 82 USPQ2d at 1396.

The difference between the prior art memory cell disclosed by Nemati et al. and the claimed device is that, where the claim(s) requires an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode, Nemati et al.'s memory cell includes an N-P-N-P negative resistance thyristor. However, Baba discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Baba. The question is, taking into account the high level of education, skill, and creativity of

Art Unit: 2826

one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claim 12 by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for Nemati et al.'s N-P-N-P negative resistance thyristor?

To base a claim rejection on the framework of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

- (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;
- (2) a finding that the substituted components and their functions were known in the art;
- (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and
- (4) whatever additional findings based on the Graham factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Nemati et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode) for other components (a N-P-N-P negative resistance thyristor). Baba discloses that the substituted components and their functions were known in the art. Further, Baba discloses that those of skill in the art were familiar with a method of combining the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode with a memory cell very similar to Nemati et al.'s memory cell. From the similarities between the I/V response curves of Baba's P-I-N negative resistance diode and the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell, one of skill in the art would have been able to conclude that Baba's P-I-N negative resistance diode would have been substitutable for the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell) that Baba's P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Nemati et al.'s memory cell, and that in said combination Nemati et al.'s memory cell would continue functioning in the manner disclosed by

Art Unit: 2826

Nemati et al. It would therefore have been obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell.

With regard to claim 13, the scope and content of the prior art includes, in the Nemati et al. disclosure, a description of a memory cell, comprising an n-channel access transistor 12 on a semiconductor-on-insulator (note figure 6a) substrate, the n-channel access transistor 12 having a floating body (part of second diffusion 24) and a n-type first diffusion region (not numbered; seen directly under bit line 18) connected to a bit line 18 and an n-type second diffusion region 24, the n-type second diffusion region 24 to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) n/p diode 10 having an n-type anode (the unnumbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19) connected to a diode reference potential line 19 and a p-type cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24) in contact with the n-type second diffusion region 24, said cell being reasonable capable, should circumstances arise, of performing the function of enhancing diode 10 switching with intentionally-generated charges in the floating body of the access transistor 12. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al. Note, column 7 lines 16-31, that Nemati et al. did not explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. "[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." CATAN, 83 USPQ2d at 1573, quoting KSR, 127 S.Ct. at 1741, 82 USPQ2d at 1396.

The difference between the prior art memory cell disclosed by Nemati et al. and the claimed device is that, where the claim(s) requires an NDR diode including an intrinsic

Art Unit: 2826

region between the anode and the cathode to assist with stabilizing the state of the NDR diode, Nemati et al.'s memory cell includes an N-P-N-P negative resistance thyristor. However, Baba discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Baba. The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claim 13 by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for Nemati et al.'s N-P-N-P negative resistance thyristor?

To base a claim rejection on the framework of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

- (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;
- (2) a finding that the substituted components and their functions were known in the art;
- (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and
- (4) whatever additional findings based on the Graham factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Nemati et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode) for other components (a N-P-N-P negative resistance thyristor). Baba discloses that the substituted components and their functions were known in the art. Further, Baba discloses that those of skill in the art were familiar with a method of combining the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode with a memory cell very similar to Nemati et al.'s memory cell. From the similarities between the I/V response curves of Baba's P-I-N negative resistance diode and the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell, one of skill in the art would have been able to conclude that Baba's P-I-N negative resistance diode would have been substitutable for

the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell) that Baba's P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Nemati et al.'s memory cell, and that in said combination Nemati et al.'s memory cell would continue functioning in the manner disclosed by Nemati et al. It would therefore have been obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell.

With regard to claim 14, the scope and content of the prior art includes, in the Nemati et al. disclosure, a description of a memory cell, comprising a p-channel access transistor 12 on a semiconductor-on-insulator (note figure 6a) substrate, the p-channel access transistor 12 having a floating body (part of second diffusion 24) and a p-type first diffusion region (not numbered; seen directly under bit line 18) connected to a bit line 18 and a p-type second diffusion region 24, the p-type second diffusion region 24 to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) n/p diode 10 having an n-type anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19) connected to a diode reference potential line 19 and a p-type cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24) in contact with the n-type second diffusion region 24, said cell being reasonable capable, should circumstances arise, of performing the function of enhancing diode 10 switching with intentionally-generated charges in the floating body of the access transistor 12. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al. Note, column 7 lines 16-31, that Nemati et al. did not explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. "[T]he analysis need not seek out precise teachings directed to

Art Unit: 2826

the specific subject matter of the challenged claim, for a court can take account of the inferences and

The difference between the prior art memory cell disclosed by Nemati et al. and the claimed device is that, where the claim(s) requires an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode, Nemati et al.'s memory cell includes an N-P-N-P negative resistance thyristor. However, Baba discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Baba. The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claim 14 by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for Nemati et al.'s N-P-N-P negative resistance thyristor?

To base a claim rejection on the framework of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

- (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;
- (2) a finding that the substituted components and their functions were known in the art;
- (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and
- (4) whatever additional findings based on the Graham factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Nemati et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode) for other components (a N-P-N-P negative resistance thyristor). Baba discloses that the substituted components and their functions were known in the art. Further, Baba discloses that those of skill in the art were familiar with a method of combining the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode with a memory cell very

Art Unit: 2826

similar to Nemati et al.'s memory cell. From the similarities between the I/V response curves of Baba's P-I-N negative resistance diode and the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell, one of skill in the art would have been able to conclude that Baba's P-I-N negative resistance diode would have been substitutable for the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell) that Baba's P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Nemati et al.'s memory cell, and that in said combination Nemati et al.'s memory cell would continue functioning in the manner disclosed by Nemati et al. It would therefore have been obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell.

With regard to claim 15, the scope and content of the prior art includes, in the Nemati et al. disclosure, a description of a memory cell, comprising an n-channel access transistor 12 on a semiconductor-on-insulator (note figure 6a) substrate, the p-channel access transistor 12 having a floating body (part of second diffusion 24) and a n-type first diffusion region (not numbered; seen directly under bit line 18) connected to a bit line 18 and an n-type second diffusion region 24, the n-type second diffusion region 24 to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) p/n diode 10 having a p-type anode (the unnumbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19) connected to a diode reference potential line 19 and an n-type cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24) formed with the n-type second diffusion region 24, said cell being reasonable capable, should circumstances arise, of performing the function of enhancing diode 10 switching with intentionally-generated charges in the floating body of the access transistor 12. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al. Note, column 7 lines 16-31, that Nemati et al. did not explicitly

Art Unit: 2826

describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. "[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and

The difference between the prior art memory cell disclosed by Nemati et al. and the claimed device is that, where the claim(s) requires an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode, Nemati et al.'s memory cell includes an N-P-N-P negative resistance thyristor. However, Baba discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Baba. The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claim 15 by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for Nemati et al.'s N-P-N-P negative resistance thyristor?

To base a claim rejection on the framework of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

- (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;
- (2) a finding that the substituted components and their functions were known in the art;
- (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and
- (4) whatever additional findings based on the Graham factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Nemati et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode) for other components (a N-P-N-P negative resistance thyris-

tor). Baba discloses that the substituted components and their functions were known in the art. Further, Baba discloses that those of skill in the art were familiar with a method of combining the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode with a memory cell very similar to Nemati et al.'s memory cell. From the similarities between the I/V response curves of Baba's P-I-N negative resistance diode and the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell, one of skill in the art would have been able to conclude that Baba's P-I-N negative resistance diode would have been substitutable for the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell) that Baba's P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Nemati et al.'s memory cell, and that in said combination Nemati et al.'s memory cell would continue functioning in the manner disclosed by Nemati et al. It would therefore have been obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell.

With regard to claim 16, the scope and content of the prior art includes, in the Nemati et al. disclosure, a description of a memory cell, comprising a p-channel access transistor 12 on a semiconductor-on-insulator (note figure 6a) substrate, the p-channel access transistor 12 having a floating body (part of second diffusion 24) and a p-type first diffusion region (not numbered; seen directly under bit line 18) connected to a bit line 18 and a p-type second diffusion region 24, the p-type second diffusion region 24 to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) p/n diode 10 having a p-type anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19) connected to a diode reference potential line 19 and an n-type cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24) formed with the n-type second diffusion region 24, said cell being reasonable capable, should

Art Unit: 2826

circumstances arise, of performing the function of enhancing diode 10 switching with intentionally-generated charges in the floating body of the access transistor 12. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al. Note, column 7 lines 16-31, that Nemati et al. did not explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. “[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and

The difference between the prior art memory cell disclosed by Nemati et al. and the claimed device is that, where the claim(s) requires an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode, Nemati et al.’s memory cell includes an N-P-N-P negative resistance thyristor. However, Baba discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Baba. The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claim 16 by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for Nemati et al.’s N-P-N-P negative resistance thyristor?

To base a claim rejection on the framework of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

- (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;
- (2) a finding that the substituted components and their functions were known in the art;
- (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and
- (4) whatever additional findings based on the Graham factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Nemati et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode) for other components (a N-P-N-P negative resistance thyristor). Baba discloses that the substituted components and their functions were known in the art. Further, Baba discloses that those of skill in the art were familiar with a method of combining the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode with a memory cell very similar to Nemati et al.'s memory cell. From the similarities between the I/V response curves of Baba's P-I-N negative resistance diode and the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell, one of skill in the art would have been able to conclude that Baba's P-I-N negative resistance diode would have been substitutable for the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell) that Baba's P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Nemati et al.'s memory cell, and that in said combination Nemati et al.'s memory cell would continue functioning in the manner disclosed by Nemati et al. It would therefore have been obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell.

With regard to claim 17, the scope and content of the prior art includes, in the Nemati et al. disclosure, a description of a memory cell, comprising an access transistor 12 on a semiconductor-on-insulator (note figure 6a) substrate, the access transistor 12 having a floating body (part of second diffusion 24) and a first diffusion region (not numbered; seen directly under bit line 18) connected to a bit line 18 and a second diffusion region 24, the second diffusion region 24 to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) diode 10 connected between the second diffusion region 24 of the access transistor 12 and a diode refer-

Art Unit: 2826

ence potential line 19, the diode 10 having an anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19) and an n-type cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24) formed with the n-type second diffusion region 24, said cell being reasonable capable, should circumstances arise, of performing the function of enhancing diode 10 switching with intentionally-generated charges in the floating body of the access transistor 12. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al. Note, column 7 lines 16-31, that Nemati et al. did not explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. "[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and

The difference between the prior art memory cell disclosed by Nemati et al. and the claimed device is that, where the claim(s) requires an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode, Nemati et al.'s memory cell includes an N-P-N-P negative resistance thyristor. However, Baba discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Baba. The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claim 18 by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for Nemati et al.'s N-P-N-P negative resistance thyristor?

To base a claim rejection on the framework of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

- (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;

Art Unit: 2826

- (2) a finding that the substituted components and their functions were known in the art;
- (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and
- (4) whatever additional findings based on the Graham factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Nemati et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode) for other components (a N-P-N-P negative resistance thyristor). Baba discloses that the substituted components and their functions were known in the art. Further, Baba discloses that those of skill in the art were familiar with a method of combining the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode with a memory cell very similar to Nemati et al.'s memory cell. From the similarities between the I/V response curves of Baba's P-I-N negative resistance diode and the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell, one of skill in the art would have been able to conclude that Baba's P-I-N negative resistance diode would have been substitutable for the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell) that Baba's P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Nemati et al.'s memory cell, and that in said combination Nemati et al.'s memory cell would continue functioning in the manner disclosed by Nemati et al. It would therefore have been obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell.

With regard to claim 18, the scope and content of the prior art includes, in the Nemati et al. disclosure, a description of a memory cell, comprising an access transistor 12 on a semiconductor-on-insulator (note figure 6a) substrate, the access transistor 12 having a floating body (part of second diffusion 24) and a first diffusion region (not num-

Art Unit: 2826

bered; seen directly under bit line 18) connected to a bit line 18 and a second diffusion region 24, the second diffusion region 24 to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) diode 10 connected between the second diffusion region 24 of the access transistor 12 and a diode reference potential line 19, the diode 10 having an anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19) and a cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24), the diode 10 being vertically oriented over the access transistor 12, said cell being reasonable capable, should circumstances arise, of performing the function of enhancing diode 10 switching with intentionally-generated charges in the floating body of the access transistor 12. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al. Note, column 7 lines 16-31, that Nemati et al. did not explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. "[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and

The difference between the prior art memory cell disclosed by Nemati et al. and the claimed device is that, where the claim(s) requires an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode, Nemati et al.'s memory cell includes an N-P-N-P negative resistance thyristor. However, Baba discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Baba. The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claim 18 by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for Nemati et al.'s N-P-N-P negative resistance thyristor?

Art Unit: 2826

To base a claim rejection on the framework of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

- (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;
- (2) a finding that the substituted components and their functions were known in the art;
- (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and
- (4) whatever additional findings based on the Graham factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Nemati et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode) for other components (a N-P-N-P negative resistance thyristor). Baba discloses that the substituted components and their functions were known in the art. Further, Baba discloses that those of skill in the art were familiar with a method of combining the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode with a memory cell very similar to Nemati et al.'s memory cell. From the similarities between the I/V response curves of Baba's P-I-N negative resistance diode and the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell, one of skill in the art would have been able to conclude that Baba's P-I-N negative resistance diode would have been substitutable for the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell) that Baba's P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Nemati et al.'s memory cell, and that in said combination Nemati et al.'s memory cell would continue functioning in the manner disclosed by Nemati et al. It would therefore have been obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the

Art Unit: 2826

NDR diode taught by Baba for the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell.

With regard to claim 19, the scope and content of the prior art includes, in the Nemati et al. disclosure, a description of a memory cell, comprising an access transistor 12 on a semiconductor-on-insulator (note figure 6a) substrate, the access transistor 12 having a floating body (part of second diffusion 24) and a first diffusion region (not numbered; seen directly under bit line 18) connected to a bit line 18 and a second diffusion region 24, the second diffusion region 24 to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) diode 10 connected between the second diffusion region 24 of the access transistor 12 and a diode reference potential line 19, the diode 10 having an anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19) and a cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24), the diode 10 being vertically oriented over the access transistor 12, said cell being reasonable capable, should circumstances arise, of performing the function of enhancing diode 10 switching with intentionally-generated charges in the floating body of the access transistor 12. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al. Note, column 7 lines 16-31, that Nemati et al. did not explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. "[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and

The difference between the prior art memory cell disclosed by Nemati et al. and the claimed device is that, where the claim(s) requires an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode, Nemati et al.'s memory cell includes an N-P-N-P negative resistance thyristor. However, Baba discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Baba.

Art Unit: 2826

The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claim 19 by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for Nemati et al.'s N-P-N-P negative resistance thyristor?

To base a claim rejection on the framework of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

- (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;
- (2) a finding that the substituted components and their functions were known in the art;
- (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and
- (4) whatever additional findings based on the Graham factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Nemati et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (an NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode) for other components (a N-P-N-P negative resistance thyristor). Baba discloses that the substituted components and their functions were known in the art. Further, Baba discloses that those of skill in the art were familiar with a method of combining the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode with a memory cell very similar to Nemati et al.'s memory cell. From the similarities between the I/V response curves of Baba's P-I-N negative resistance diode and the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell, one of skill in the art would have been able to conclude that Baba's P-I-N negative resistance diode would have been substitutable for the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell) that Baba's P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Nemati et al.'s memory cell, and that in said combina-

Art Unit: 2826

tion Nemati et al.'s memory cell would continue functioning in the manner disclosed by Nemati et al. It would therefore have been obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the NDR diode including an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode taught by Baba for the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell.

With regard to claims 20-28, 30, and 31, the scope and content of the prior art includes, in the Nemati et al. disclosure, a description of a memory cell, comprising an access transistor 12, including a body region 16; a first diffusion region (not numbered; seen directly under bit line 18) electrically connected to a bit line 18; a second diffusion region 24 separated from the first diffusion region by a channel area in the body region 16; a gate 14 separated from the channel area by a gate insulator (not numbered; seen under gate 14), the gate 14 electrically connected to a word line 14; a Negative Differential Resistance (NDR) diode 10, including an anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19) and a cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24), the diode 10 being connected between the second diffusion region 24 and a diode reference potential line 19, said cell being reasonable capable, should circumstances arise, of performing the function of operating to store and sense a charge in the second diffusion region 24 that may be representative of a memory state, wherein the access transistor 12 may include an n-channel transistor or a p-channel transistor, wherein the diode 10 may include a p/n diode 10 having a p-type anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19) and an n-type cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24), the p/n diode 10 may include a p⁺/n⁺ diode 10 having a p⁺ anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19) and an n⁺ cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24), the diode 10 may include an n/p diode 10 having an n-type anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19) and a p-type cathode (part of diode 10 that is adjacent to and sometimes con-

tiguous with node 24), or an n+/p diode 10 having an n+ anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19) and a p cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24), wherein the diode 10 may include a laterally-oriented or vertically-oriented diode 10 or a gate-controlled diode 10 to enhance switching performance and reduce standby power, and the access transistor 12 may be on a semiconductor-on-insulator (note figure 6a) or bulk semiconductor (note figure 6) substrate. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al. Note, column 7 lines 16-31, that Nemati et al. did not explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. “[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and

The difference between the prior art memory cell disclosed by Nemati et al. and the device of claims 20-28, 30, and 31 is that, where the claim(s) requires an NDR diode including an intrinsic region between the anode and the cathode, Nemati et al.’s memory cell includes an N-P-N-P negative resistance thyristor. However, Baba discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Baba. The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claims 20-28, 30, and 31 by substituting the NDR diode including an intrinsic region between the anode and the cathode taught by Baba for Nemati et al.’s N-P-N-P negative resistance thyristor?

To base a claim rejection on the framework of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

- (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;

Art Unit: 2826

- (2) a finding that the substituted components and their functions were known in the art;
- (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and
- (4) whatever additional findings based on the Graham factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Nemati et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (a NDR diode including an intrinsic region between the anode and the cathode) for other components (a N-P-N-P negative resistance thyristor). Baba discloses that the substituted components and their functions were known in the art. Further, Baba discloses that those of skill in the art were familiar with a method of combining a NDR diode including an intrinsic region between the anode and the cathode with a memory cell very similar to Nemati et al.'s memory cell. From the similarities between the I/V response curves of Baba's P-I-N negative resistance diode and the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell, one of skill in the art would have been able to conclude that Baba's P-I-N negative resistance diode would have been substitutable for the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell) that Baba's P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Nemati et al.'s memory cell, and that in said combination Nemati et al.'s memory cell would continue functioning in the manner disclosed by Nemati et al. It would therefore have been obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the NDR diode including an intrinsic region between the anode and the cathode taught by Baba for the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell.

With regard to claim 29, the scope and content of the prior art includes, in the Nemati et al. disclosure, a description of a memory cell, comprising an access transistor 12, including a body region 16; a first diffusion region (not numbered; seen directly under bit line 18) electrically connected to a bit line 18; a second diffusion region 24 separated from the first diffusion region by a channel area in the body region 16; a gate 14 separated from the channel area by a gate insulator (not numbered; seen under gate

Art Unit: 2826

14), the gate 14 electrically connected to a word line 14 ; a Negative Differential Resistance (NDR) diode 10, including an anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19) and a cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24), the diode 10 being connected between the second diffusion region 24 and a diode reference potential line 19, said cell being reasonable capable, should circumstances arise, of performing the function of operating to store and sense a charge in the second diffusion region 24 that may be representative of a memory state. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al. Note, column 7 lines 16-31, that Nemati et al. did not explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. “[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and

The difference between the prior art memory cell disclosed by Nemati et al. and the claimed device is that, where claim 29 requires an NDR diode formed so as to include an intrinsic region, between the anode and the cathode of the NDR diode, having a desired geometry to assist with stabilizing the state of the NDR diode, Nemati et al.’s memory cell includes an N-P-N-P negative resistance thyristor. However, Baba discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14, having a desired geometry to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Baba. The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claim 29 by substituting the NDR diode formed so as to include an intrinsic region, between the anode and the cathode of the NDR diode, having a desired geometry to assist with stabilizing the state of the NDR diode taught by Baba for Nemati et al.’s N-P-N-P negative resistance thyristor?

Art Unit: 2826

To base a claim rejection on the framework of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

- (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;
- (2) a finding that the substituted components and their functions were known in the art;
- (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and
- (4) whatever additional findings based on the Graham factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Nemati et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (a NDR diode formed so as to include an intrinsic region, between the anode and the cathode of the NDR diode, having a desired geometry to assist with stabilizing the state of the NDR diode) for other components (a N-P-N-P negative resistance thyristor). Baba discloses that the substituted components and their functions were known in the art. Further, Baba discloses that those of skill in the art were familiar with a method of combining the NDR diode formed so as to include an intrinsic region, between the anode and the cathode of the NDR diode, having a desired geometry to assist with stabilizing the state of the NDR diode with a memory cell very similar to Nemati et al.'s memory cell. From the similarities between the I/V response curves of Baba's P-I-N negative resistance diode and the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell, one of skill in the art would have been able to conclude that Baba's P-I-N negative resistance diode would have been substitutable for the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell) that Baba's P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Nemati et al.'s memory cell, and that in said combination Nemati et al.'s memory cell would continue functioning in the manner disclosed by Nemati et al. It would therefore have been obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the NDR diode formed so as to include an intrinsic region, between

Art Unit: 2826

the anode and the cathode of the NDR diode, having a desired geometry to assist with stabilizing the state of the NDR diode taught by Baba for the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell.

With regard to claims 33-41, the scope and content of the prior art includes, in the Nemati et al. disclosure, a description of a memory cell, comprising an access transistor 12 formed in a bulk semiconductor (note figure 6) structure, the access transistor 12 including a first diffusion region (not numbered; seen directly under bit line 18) separated from a second diffusion region 24 by a channel region, and further including a gate 14 separated from the channel region by a gate insulator (not numbered; seen under gate 14), wherein the first diffusion region may be connected to a bit line 18 and the gate 14 may be connected to a first word line 14; and a gate-controlled Negative Differential Resistance (NDR) diode 10 connected between a reference potential line 19 and the second diffusion region 24, the diode 10 including an anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19), a cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24), and a diode gate connected to a second word line 20, wherein the gate-controlled diode 10 may include a laterally-oriented diode 10 positioned over the access transistor 12, or a vertically-oriented diode 10, the first and second diffusion regions of the access transistor 12 include n-type or p-type dopants; and the gate-controlled diode 10 may include a p/n or n/p diode 10 having a p-type or n-type anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19) connected to the reference potential line 19 and an n-type or p-type cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24) formed with the second diffusion region 24. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al. Note, column 7 lines 16-31, that Nemati et al. did not explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. "[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged

Art Unit: 2826

claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.”

The applicant’s claim 36 does not distinguish over the Nemati et al. reference regardless of the process used to form the lateral-orientated diode, because only the final product is relevant, not the recited process of using raised source/drain techniques and metal-induced-lateral crystallization techniques. See *SmithKline Beecham Corp. v. Apotex Corp.*, 78 USPQ2d 1097 (Fed. Cir, 2006 (“While the process set forth in the product-by-process claim may be new, that novelty can only be captured by obtaining a process claim.”))

The difference between the prior art memory cell disclosed by Nemati et al. and the claimed device is that, where claims 33-41 require an NDR diode formed so as to include an intrinsic region, between the anode and the cathode of the NDR diode, having a desired geometry to assist with stabilizing the state of the NDR diode and operatively positioned to enhance switching performance, Nemati et al.’s memory cell includes an N-P-N-P negative resistance thyristor. However, Baba discloses a P-I-N negative resistance diode 10 formed so as to include an intrinsic region 13, between an anode 11 and a cathode 14 of the diode, having a desired geometry to assist with stabilizing the state of the diode and be operatively positioned to enhance switching performance. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Baba. The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claims 33-41 by substituting the NDR diode formed so as to include an intrinsic region, between the anode and the cathode of the NDR diode, having a desired geometry to assist with stabilizing the state of the NDR diode and operatively positioned to enhance switching performance taught by Baba for Nemati et al.’s N-P-N-P negative resistance thyristor?

To base a claim rejection on the framework of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

- (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;
- (2) a finding that the substituted components and their functions were known in the art;

Art Unit: 2826

(3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and

(4) whatever additional findings based on the Graham factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Nemati et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (a NDR diode formed so as to include an intrinsic region, between the anode and the cathode of the NDR diode, having a desired geometry to assist with stabilizing the state of the NDR diode and operatively positioned to enhance switching performance) for other components (a N-P-N-P negative resistance thyristor). Baba discloses that the substituted components and their functions were known in the art. Further, Baba discloses that those of skill in the art were familiar with a method of combining the NDR diode formed so as to include an intrinsic region, between the anode and the cathode of the NDR diode, having a desired geometry to assist with stabilizing the state of the NDR diode and operatively positioned to enhance switching performance with a memory cell very similar to Nemati et al.'s memory cell. From the similarities between the I/V response curves of Baba's P-I-N negative resistance diode and the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell, one of skill in the art would have been able to conclude that Baba's P-I-N negative resistance diode would have been substitutable for the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell) that Baba's P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Nemati et al.'s memory cell, and that in said combination Nemati et al.'s memory cell would continue functioning in the manner disclosed by Nemati et al. It would therefore have been obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the NDR diode formed so as to include an intrinsic region, between the anode and the cathode of the NDR diode, having a desired geometry to assist with stabilizing the state of the NDR diode and operatively positioned to enhance switching performance taught by Baba for the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell.

Art Unit: 2826

With regard to claims 42-53, the scope and content of the prior art includes, in the Nemati et al. disclosure, a description of a memory cell, comprising an semiconductor-on-insulator (note figure 6a) (SOI) structure, including an SOI access transistor 12 including a first diffusion region (not numbered; seen directly under bit line 18) separated from a second diffusion region 24 by a channel region, and further including a gate 14 separated from the channel region by a gate insulator (not numbered; seen under gate 14), wherein the first diffusion region may be connected to a bit line 18 and the gate 14 may be connected to a first word line 14 ; and a Negative Differential Resistance (NDR) diode 10 connected between the second diffusion region 24 and a reference potential line 19, the diode 10 including an anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19), a cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24), a diode gate connected to a second word line 20; the anode and the cathode having a desired geometry to store a charge indicative of a memory state and being operably positioned with respect to the diode gate 20, wherein the diode 10 may include a lateral-oriented diode 10 positioned over the access transistor 12 and the SOI access transistor 12 and the lateral-oriented diode 10 may be formed in a semiconductor volume over a buried oxide (BOX) region, the diode 10 may include a vertical-oriented diode 10 including the second diffusion region 24 of the access transistor 12, and the first and second diffusion regions of the access transistor 12 may include n-type or p-type dopants; and the gate-controlled diode 10 may include a p/n or n/p diode 10 having an n-type or p-type anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19) connected to the reference potential line 19 and a p-type or n-type cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24) formed with the second diffusion region 24. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al. Note, column 7 lines 16-31, that Nemati et al. did not explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. "[T]he analysis need not seek out precise teachings directed to

Art Unit: 2826

the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.”

The applicant’s claim 46 does not distinguish over the Nemati et al. reference regardless of the process used to form the lateral-orientated diode, because only the final product is relevant, not the recited process of using raised source/drain techniques and metal-induced-lateral crystallization techniques. See *SmithKline Beecham Corp. v. Apotex Corp.*, 78 USPQ2d 1097 (Fed. Cir, 2006 (“While the process set forth in the product-by-process claim may be new, that novelty can only be captured by obtaining a process claim.”))

The difference between the prior art memory cell disclosed by Nemati et al. and the device of claims 42-53 is that, where the claim(s) requires an NDR diode including an intrinsic region between the anode and the cathode, Nemati et al.’s memory cell includes an N-P-N-P negative resistance thyristor. However, Baba discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Baba. The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claims 42-53 by substituting the NDR diode including an intrinsic region between the anode and the cathode taught by Baba for Nemati et al.’s N-P-N-P negative resistance thyristor?

To base a claim rejection on the framework of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

- (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;
- (2) a finding that the substituted components and their functions were known in the art;
- (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and
- (4) whatever additional findings based on the Graham factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Nemati et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (a NDR diode in-

cluding an intrinsic region between the anode and the cathode) for other components (a N-P-N-P negative resistance thyristor). Baba discloses that the substituted components and their functions were known in the art. Further, Baba discloses that those of skill in the art were familiar with a method of combining a NDR diode including an intrinsic region between the anode and the cathode with a memory cell very similar to Nemati et al.'s memory cell. From the similarities between the I/V response curves of Baba's P-I-N negative resistance diode and the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell, one of skill in the art would have been able to conclude that Baba's P-I-N negative resistance diode would have been substitutable for the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell) that Baba's P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Nemati et al.'s memory cell, and that in said combination Nemati et al.'s memory cell would continue functioning in the manner disclosed by Nemati et al. It would therefore have been obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the NDR diode including an intrinsic region between the anode and the cathode taught by Baba for the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell.

With regard to claims 54-62, the scope and content of the prior art includes, in the Nemati et al. disclosure, a description of a memory cell, comprising an access transistor 12, the access transistor 12 including a first diffusion region (not numbered; seen directly under bit line 18) separated from a second diffusion region 24 by a channel region, and further including a gate 14 separated from the channel region by a gate insulator (not numbered; seen under gate 14), wherein the first diffusion region may be connected to a bit line 18 and the gate 14 may be connected to a first word line 14 ; and a Negative Differential Resistance (NDR) p+/n+ diode 10 connected between a diode reference potential line 19 and the second diffusion region 24, the p/n diode 10 including a p+ anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19), an n+ cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24), and a diode gate connected to

Art Unit: 2826

a second word line 20, wherein the diode 10 may include a laterally-oriented or vertically-oriented diode 10 or a gate-controlled diode 10 to enhance switching performance and reduce standby power, and the access transistor 12 may include a p-channel or n-channel transistor on a semiconductor-on-insulator (note figure 6a) or bulk semiconductor (note figure 6) substrate. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al. Note, column 7 lines 16-31, that Nemati et al. did not explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. "[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and

The difference between the prior art memory cell disclosed by Nemati et al. and the claimed device is that, where claims 54-62 require an NDR diode including an intrinsic region operably positioned between an anode and a cathode, Nemati et al.'s memory cell includes an N-P-N-P negative resistance thyristor. However, Baba discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 operably positioned between an anode 11 and a cathode 14. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Baba. The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claims 54-62 by substituting the NDR diode including an intrinsic region operably positioned between an anode and a cathode taught by Baba for Nemati et al.'s N-P-N-P negative resistance thyristor?

To base a claim rejection on the framework of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

- (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;
- (2) a finding that the substituted components and their functions were known in the art;
- (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and

(4) whatever additional findings based on the Graham factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Nemati et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (a NDR diode including an intrinsic region operably positioned between an anode and a cathode) for other components (a N-P-N-P negative resistance thyristor). Baba discloses that the substituted components and their functions were known in the art. Further, Baba discloses that those of skill in the art were familiar with a method of combining the NDR diode including an intrinsic region operably positioned between an anode and a cathode with a memory cell very similar to Nemati et al.'s memory cell. From the similarities between the I/V response curves of Baba's P-I-N negative resistance diode and the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell, one of skill in the art would have been able to conclude that Baba's P-I-N negative resistance diode would have been substitutable for the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell) that Baba's P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Nemati et al.'s memory cell, and that in said combination Nemati et al.'s memory cell would continue functioning in the manner disclosed by Nemati et al. It would therefore have been obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the NDR diode including an intrinsic region operably positioned between an anode and a cathode taught by Baba for the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell.

With regard to claims 63-71, the scope and content of the prior art includes, in the Nemati et al. disclosure, a description of a memory cell, comprising an access transistor 12, the access transistor 12 including a first diffusion region (not numbered; seen directly under bit line 18) separated from a second diffusion region 24 by a channel region, and further including a gate 14 separated from the channel region by a gate insulator (not numbered; seen under gate 14), wherein the first diffusion region may be connected to a bit line 18 and the gate 14 may be connected to a first word line 14 ; and a

Art Unit: 2826

Negative Differential Resistance (NDR) n+/p diode 10 connected between a diode reference potential line 19 and the second diffusion region 24, the p/n diode 10 including an n+ anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19), a p cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24), and a diode gate connected to a second word line 20, wherein the diode 10 may include a laterally-oriented or vertically-oriented diode 10 or a gate-controlled diode 10 to enhance switching performance and reduce standby power, and the access transistor 12 may include a p-channel or n-channel transistor on a semiconductor-on-insulator (note figure 6a) or bulk semiconductor (note figure 6) substrate. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al. Note, column 7 lines 16-31, that Nemati et al. did not explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. "[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and

The difference between the prior art memory cell disclosed by Nemati et al. and the claimed device is that, where claims 63-71 require an NDR diode including an intrinsic region operably positioned between an anode and a cathode, Nemati et al.'s memory cell includes an N-P-N-P negative resistance thyristor. However, Baba discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 operably positioned between an anode 11 and a cathode 14. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Baba. The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claims 63-71 by substituting the NDR diode including an intrinsic region operably positioned between an anode and a cathode taught by Baba for Nemati et al.'s N-P-N-P negative resistance thyristor?

To base a claim rejection on the framework of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

Art Unit: 2826

- (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;
- (2) a finding that the substituted components and their functions were known in the art;
- (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and
- (4) whatever additional findings based on the Graham factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Nemati et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (a NDR diode including an intrinsic region operably positioned between an anode and a cathode) for other components (a N-P-N-P negative resistance thyristor). Baba discloses that the substituted components and their functions were known in the art. Further, Baba discloses that those of skill in the art were familiar with a method of combining the NDR diode including an intrinsic region operably positioned between an anode and a cathode with a memory cell very similar to Nemati et al.'s memory cell. From the similarities between the I/V response curves of Baba's P-I-N negative resistance diode and the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell, one of skill in the art would have been able to conclude that Baba's P-I-N negative resistance diode would have been substitutable for the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell) that Baba's P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Nemati et al.'s memory cell, and that in said combination Nemati et al.'s memory cell would continue functioning in the manner disclosed by Nemati et al. It would therefore have been obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the NDR diode including an intrinsic region operably positioned between an anode and a cathode taught by Baba for the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell.

With regard to claims 72-79, the scope and content of the prior art includes, in the Nemati et al. disclosure, a description of a memory device, comprising a memory array, including a plurality of memory cells in rows and columns; a number of word lines 14,

each word line 14 connected to a row of memory cells; a number of bit lines 12, each bit line 18 connected to a column of memory cells; at least one reference line 19 to provide a reference potential to the memory cells; control circuitry, including word line 14, select circuitry and bit line select circuitry to select a number of memory cells for writing and reading operations, wherein each memory cell may include an access transistor 12, including a body region 16, a first diffusion region (not numbered; seen directly under bit line 18) electrically connected to one of the bit lines 12, a second diffusion region 24 separated from the first diffusion region by a channel area in the body region 16, and a gate separated from the channel area by a gate insulator (not numbered; seen under gate 14) and electrically connected to one of the word lines 14; and a Negative Differential Resistance (NDR) gate-controlled diode 10, including an anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19) and a cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24), the diode 10 being connected between the second diffusion region 24 and a diode reference line 19, wherein the memory cell may be adapted to store a charge in the second diffusion region 24 of the access transistor 12 to indicate a stable memory state, wherein each memory cell may be on a bulk semiconductor (note figure 6) substrate, and the diode 10 may include a vertically-oriented diode 10 or a laterally-oriented diode 10 over the access transistor 12, or each memory cell may be on a semiconductor-on-insulator (note figure 6a) substrate such that the access transistor 12 has a floating body (formed from second diffusion 24), and the diode 10 may include a laterally-oriented diode 10 formed over, or at least partially in the floating body of, the access transistor 12. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al. Note, column 7 lines 16-31, that Nemati et al. did not explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. “[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.”

Art Unit: 2826

The difference between the prior art memory cell disclosed by Nemati et al. and the claimed device is that, where claims 72-79 require an NDR diode including an intrinsic region between an anode and a cathode, Nemati et al.'s memory cell includes an N-P-N-P negative resistance thyristor. However, Baba discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Baba. The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claims 72-79 by substituting the NDR diode including an intrinsic region between an anode and a cathode taught by Baba for Nemati et al.'s N-P-N-P negative resistance thyristor?

To base a claim rejection on the framework of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

- (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;
- (2) a finding that the substituted components and their functions were known in the art;
- (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and
- (4) whatever additional findings based on the Graham factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Nemati et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (a NDR diode including an intrinsic region between an anode and a cathode) for other components (a N-P-N-P negative resistance thyristor). Baba discloses that the substituted components and their functions were known in the art. Further, Baba discloses that those of skill in the art were familiar with a method of combining the NDR diode including an intrinsic region between an anode and a cathode with a memory cell very similar to Nemati et al.'s memory cell. From the similarities between the I/V response curves of Baba's P-I-N negative resistance diode and the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell, one of skill in the art would have been able to conclude that Baba's P-I-N negative resistance diode would have been substitutable for the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell. One of skill in the art would have had

Art Unit: 2826

reason to predict (based on the similarity of its functioning to the functioning of the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell) that Baba's P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Nemati et al.'s memory cell, and that in said combination Nemati et al.'s memory cell would continue functioning in the manner disclosed by Nemati et al. It would therefore have been obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the NDR diode including an intrinsic region between an anode and a cathode taught by Baba for the N-P-N-P negative resistance thyristor of Nemati et al.'s memory cell.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L. Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Sue A. Purvis, at 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

***/Thomas L. Dickey/
Primary Examiner
Art Unit 2826***